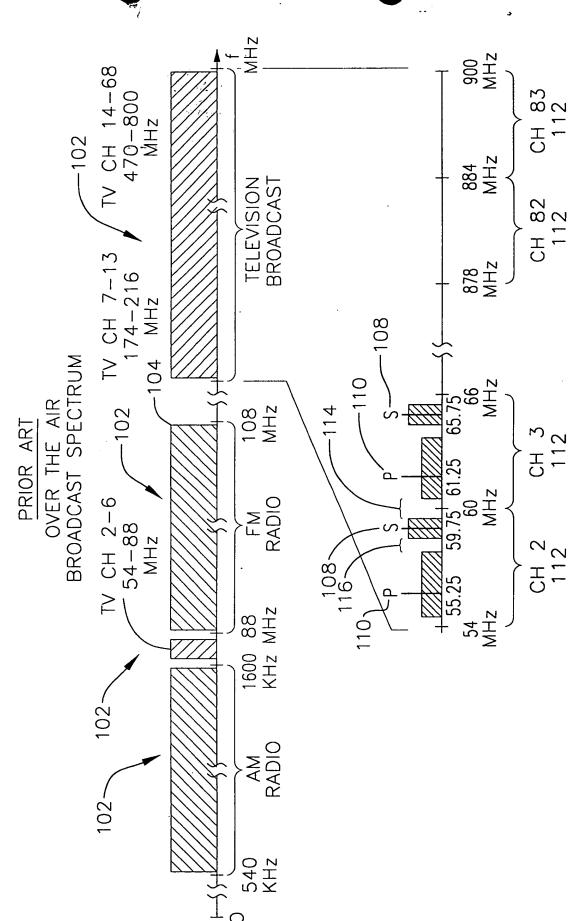
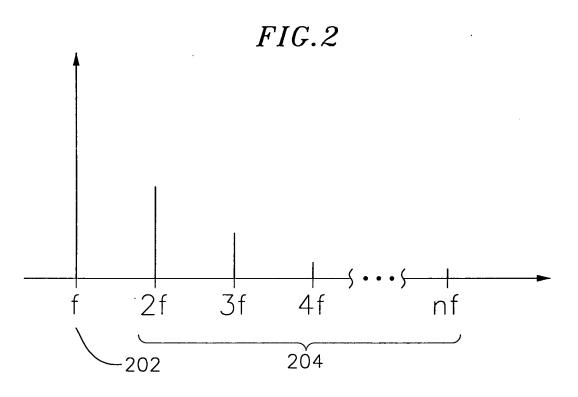
FIG. 1





DOZIOLICIECEZ

FIG.4

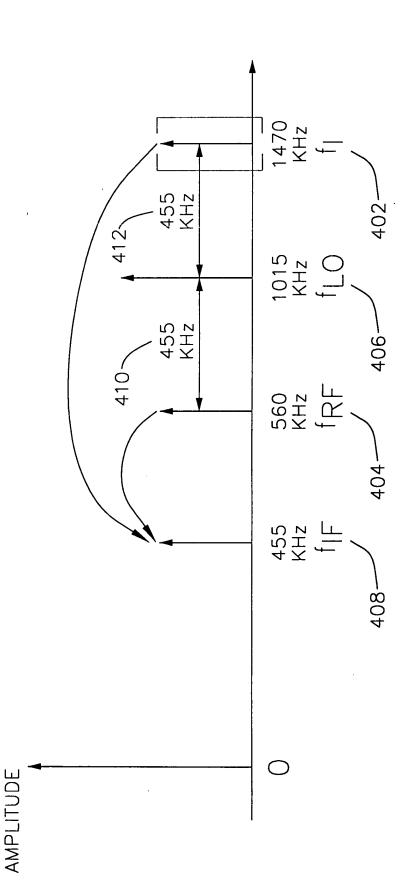
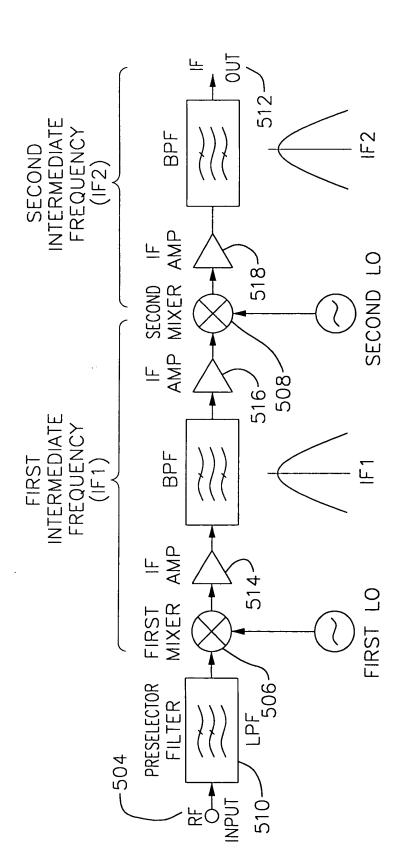
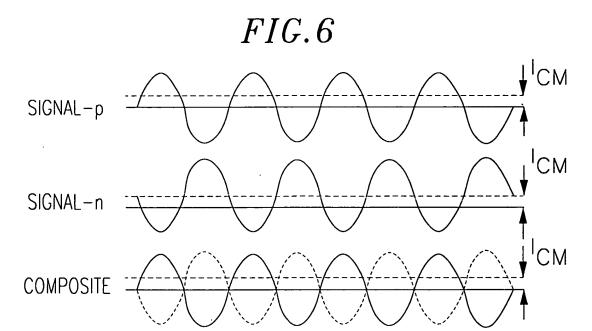


FIG.5Dual conversion receiver



IF2<RFINPUT<IF1



*FIG.* 7

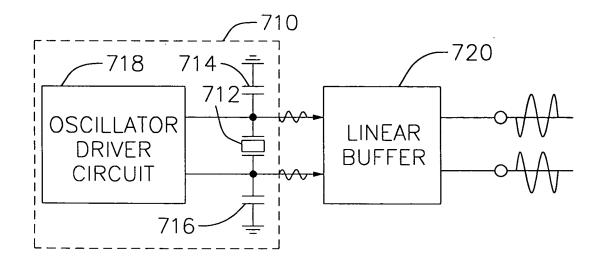
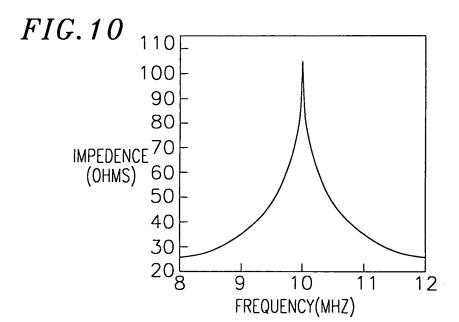
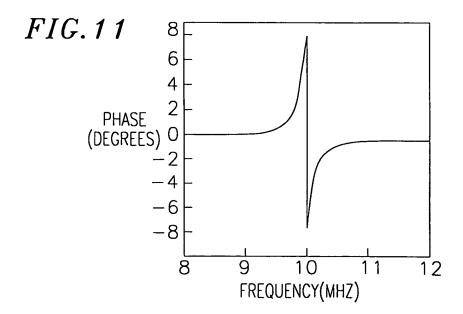


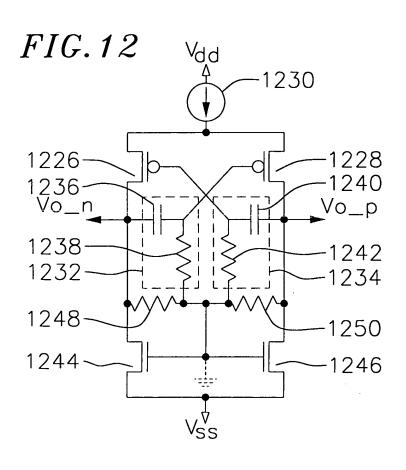




FIG.8 FIG.9 822 Co Rm







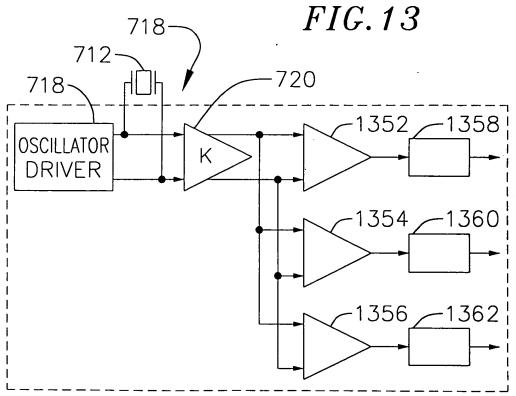
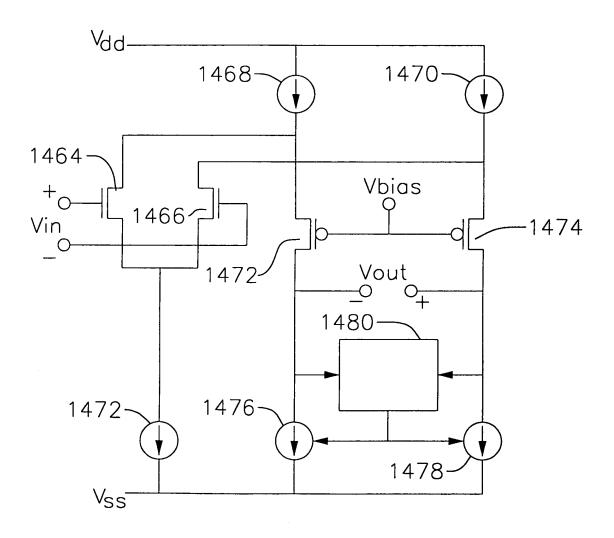
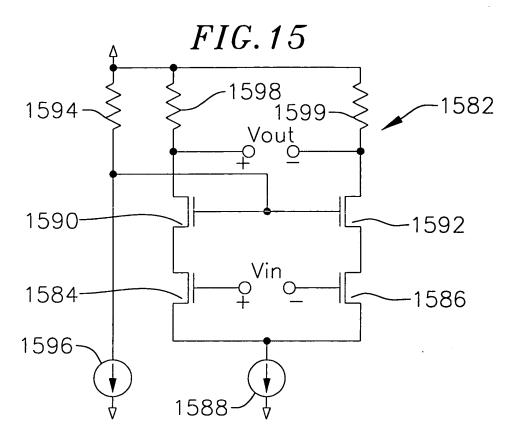


FIG. 14





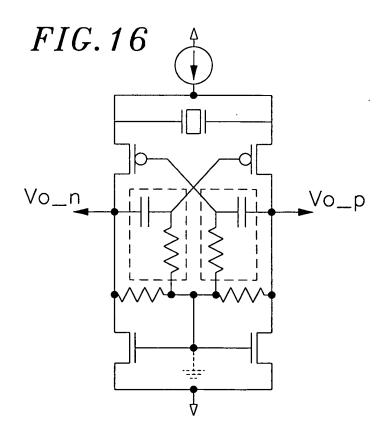


FIG. 17

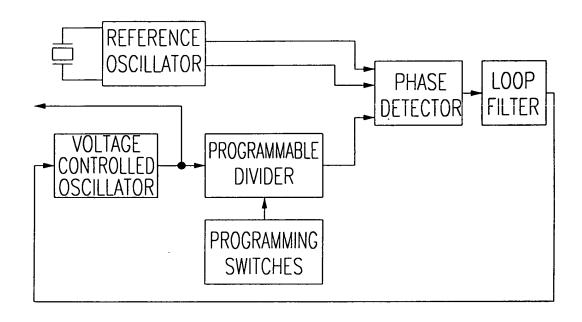
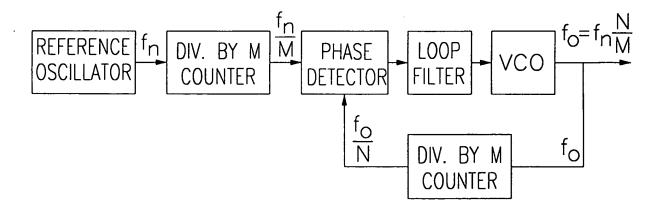


FIG. 18



## FIG. 19

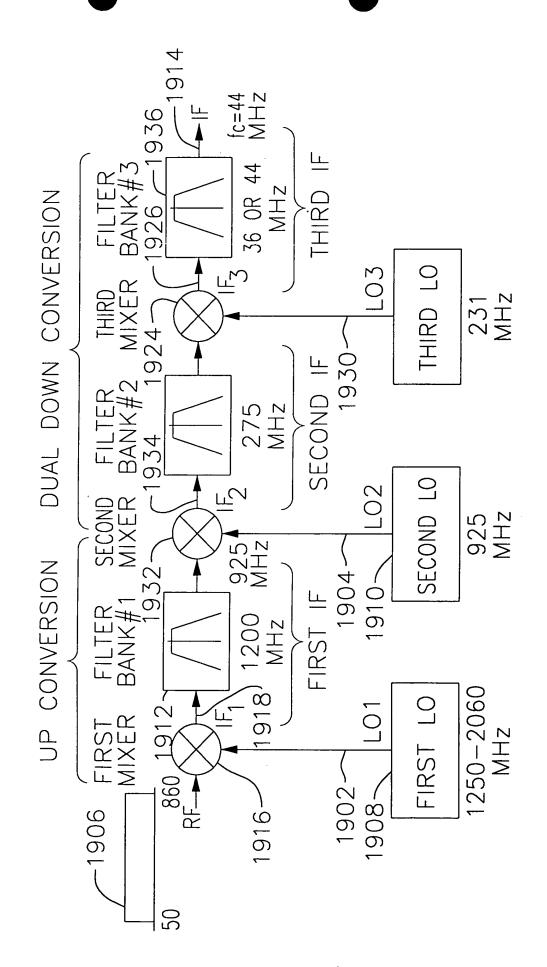
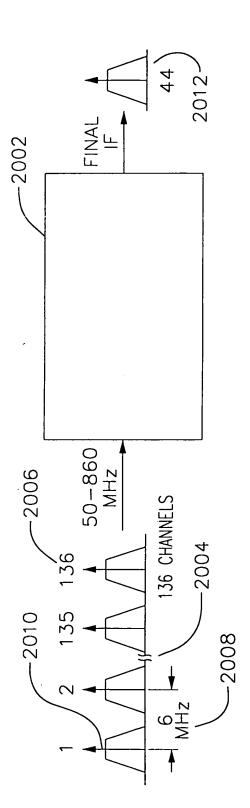


FIG.20



## DOVEDE LEGENO

PPL Xtal REFERENCE=10MHz LO-1, 10MHz FREQUENCY STEPS LO-2, 100kHz FREQUENCY STEPS

FIG.21

44MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE

• LO-2 REF=100KHz

SO DIVIDE RANGE=9216 TO 9280

128 '' 854 860		1330 11 2050 2060	1196	1196	1196 1196 1196 1197 1196 1197 1197 1197	1196 1196 1196 1196 1196 1196 1196 1196
	1320	1198	923.2	274.8	231	44.0
110 116	10 1320	1200 1204	1.8 928.0	275.2 276.0 274.8	231 232	44.0 44.0
104 1	1300 1310	1196 12	921.6 924.8	274.4 275	230 2	44.0 4
86	1300	1202	923.2 926.4	275.6 274.4	232	44.0
92	1290	1198	923.2	276.0 274.8	231	44.0
98	1290	1204	928.0	276.0	232	44.0
8	1280	1200	5 924.8	275.2	231	44.0
74	1270	1196	921.(	274.4	230	44.0
89	1270	1202	926.4	275.6	3 232	44.0
9 62	1260	1198	923.2	276 274.8 275.6	2 230.8	44.0
99	1260	1204	928.0		232	44.0
20	1250	1200	924.8	275.2	231.2	44.0
Frf (MHz)	LO-1 (MHz)	IF-1 (MH2)	LO-2 (MHz) 924.8 928.0 923.2	IF-2 (MHz)	LO-3 (MHz) 231.2	IF-3 (MHz)



PPL Xtal REFERENCE=10MHz LO-1, 10MHz FREQUENCY STEPS LO-2, 100kHz FREQUENCY STEPS

FIG.22

36MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

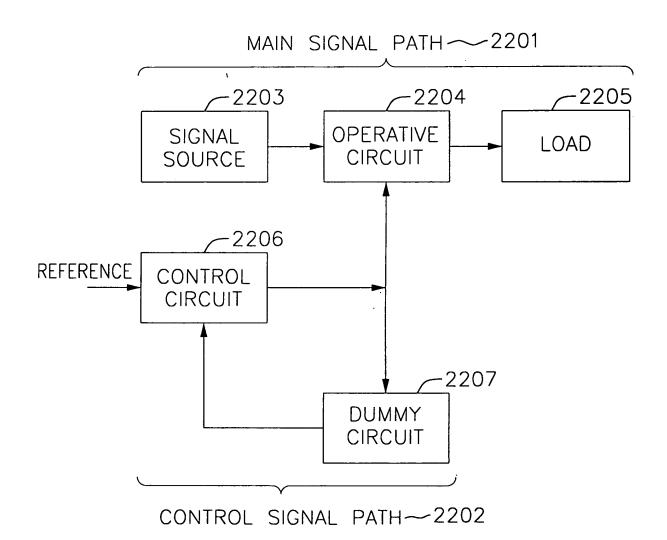
NOTE

• LO-2 REF=100KHz

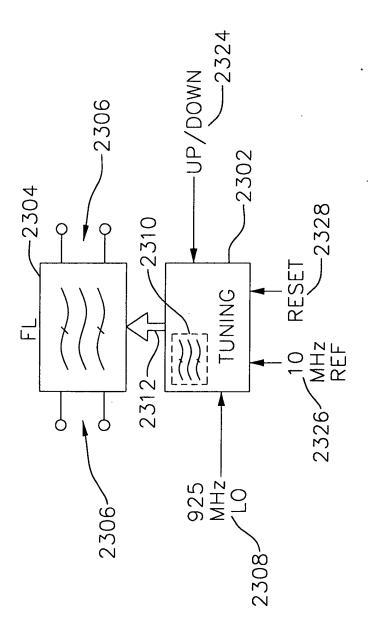
SO DIVIDE RANGE=9280 TO 9340

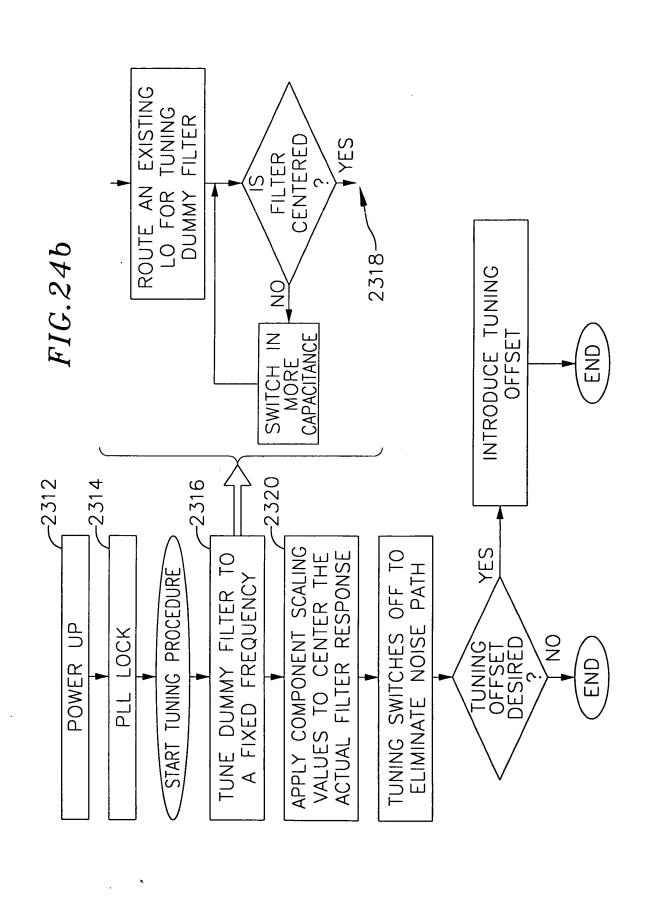
860	2060	1200	931.2	268.8	232.8	36.0
852	2050	1198	929.60	268.4	232.4	36.0
=	=	=	=	=	=	=
154	1350	1196	928.0	268.0	232.0	36.0
146	1350	1204	934	269.6	234	36.0
138	1340	1202	933	269.2	233	36.0
130	1330	1200	931	268.8	233	36.0
122	1320	1198	930	268.4	232	36.0
114	1310	1196	928.0	268.0 268.4	232	36.0
106	1310	1204	934	269.6	234	36.0
86	1300	1202	933	269.2	233	36.0
06	1290	1200	931	268.8	233	36.0
82	1280	1198	930	268.4	232	36.0
74	1270	1196	928.0	268.0	232	36.0
99	1270	1204	934.4	269.6 268.0	233.6	36.0
28	1260	1202	932.8	269.2	233.2	36.0
50	1250	1200	931.2	268.8 269.2	232.8	36.0
Frf (MHz)	LO-1 (MHz)	1F-1 (MHz)	LO-2 (MHz)	IF-2 (MHz)	LO-3 (MHz) 232.8 233.2	IF-3 (MHz)

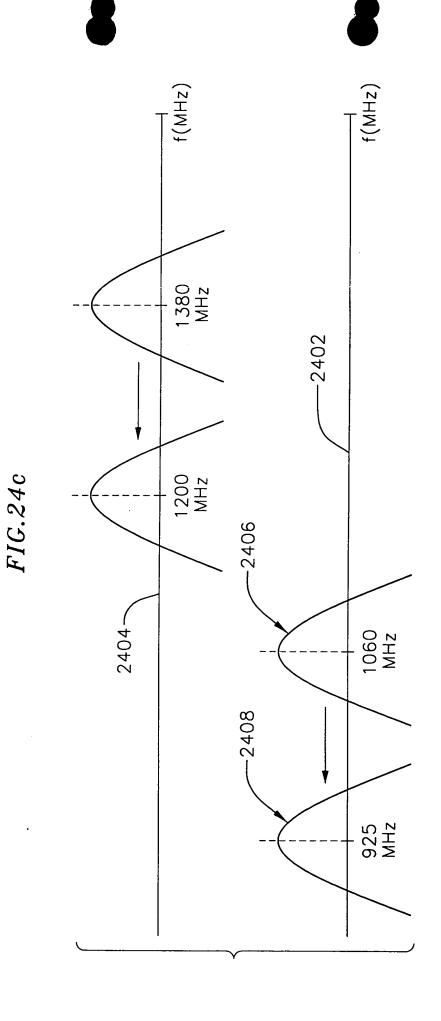
FIG.23



 $FIG.24\alpha$ 







15 -2502 -2504 RESET -2518 **\2524** 10MHz— -2516 OUTP OUTN -2530 -2510 1554ء L2520 2512 -2508 2522~ -2526 Q d <u>م</u> 9 \_z \_\_ Š <u>\_</u>Z 2510-2528-ပ 2506~ 2508 \_ Z

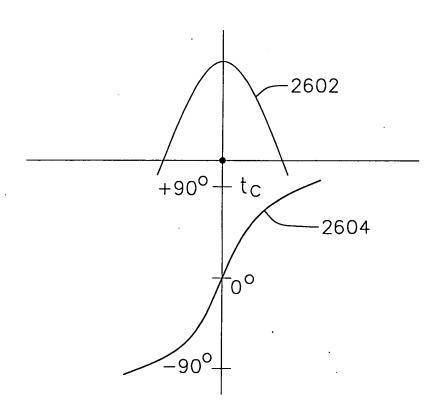
DOFFEEL CARCE

FIG.25





FIG.26



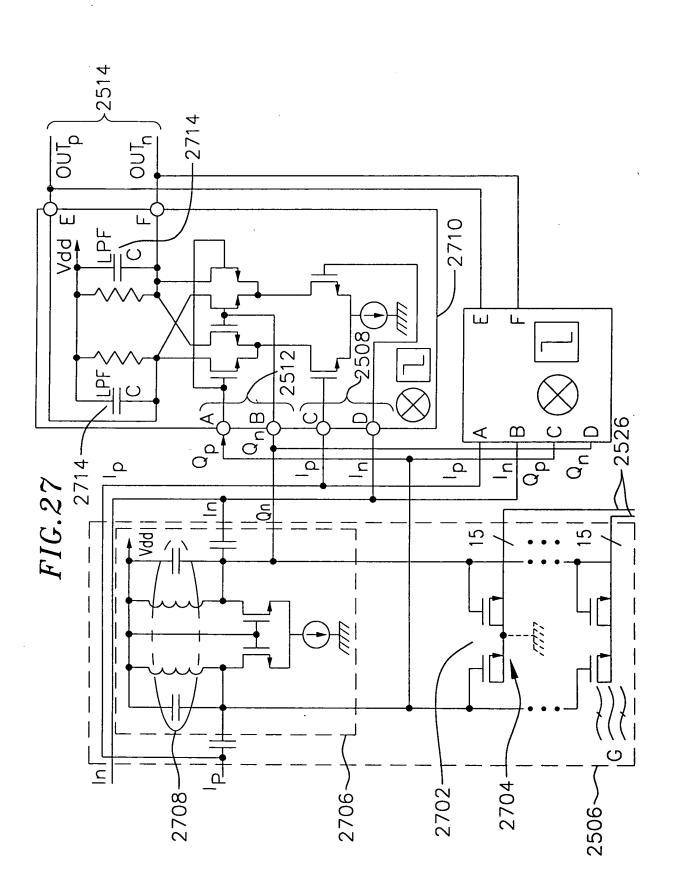
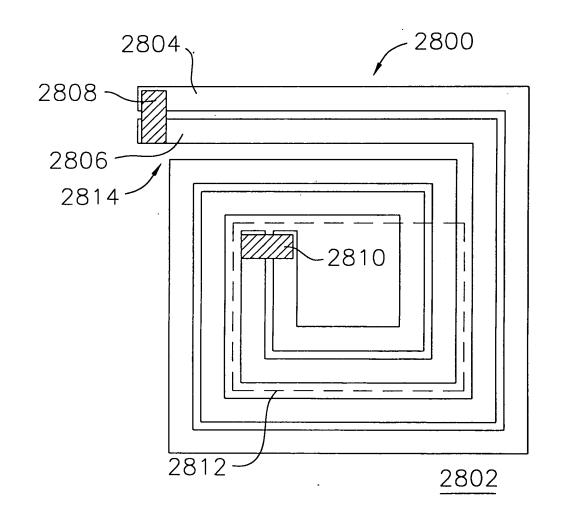
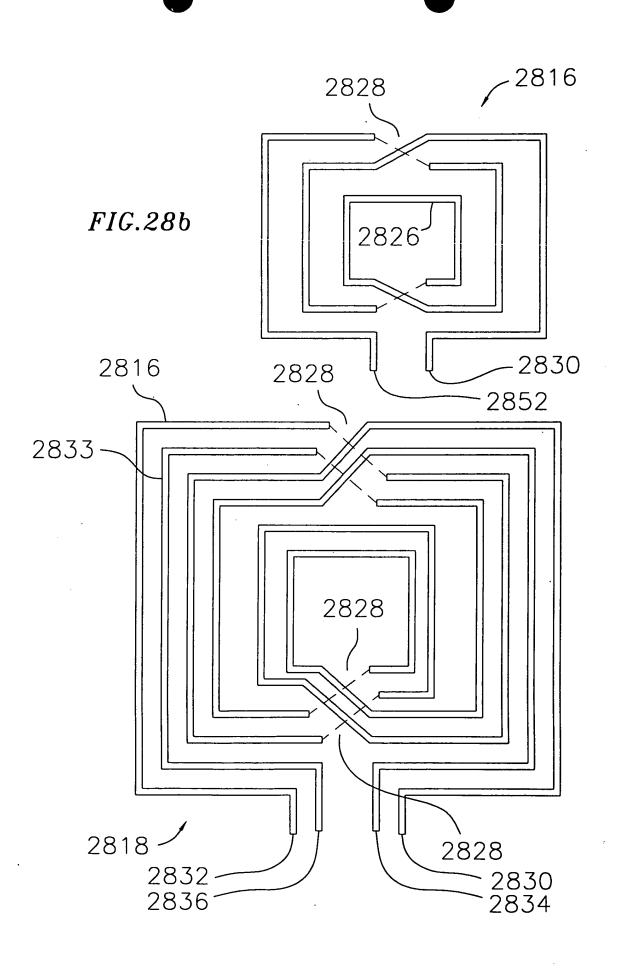


FIG.28a





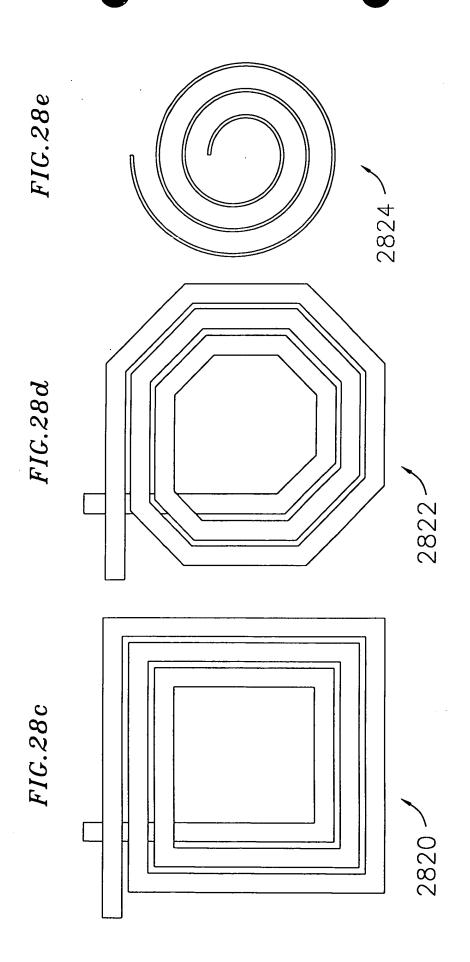


FIG.28f

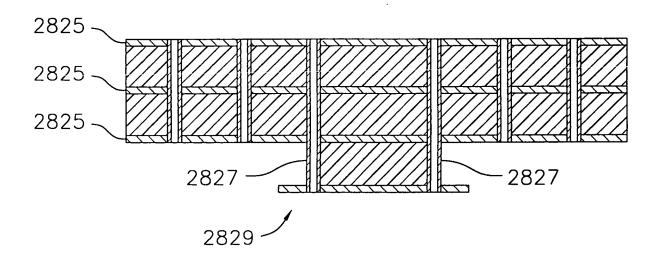


FIG.28g

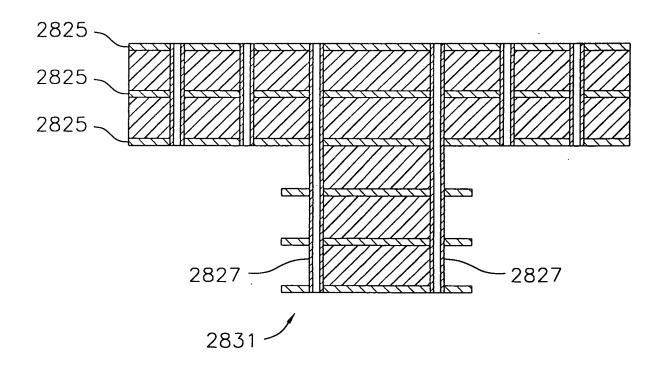


FIG.28i

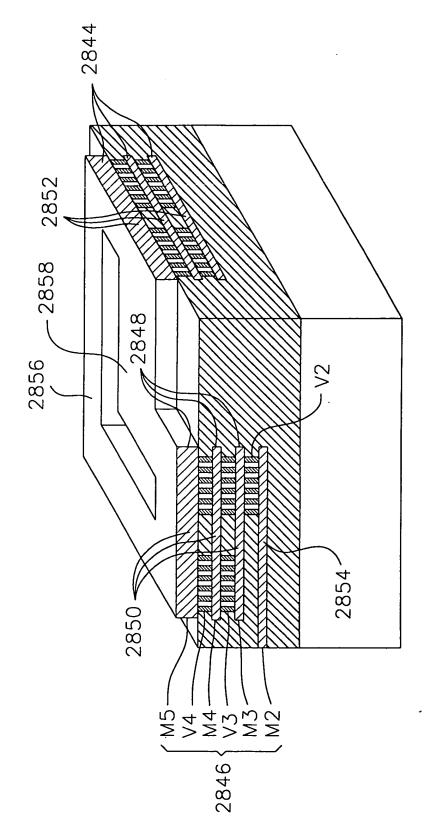


FIG.28h

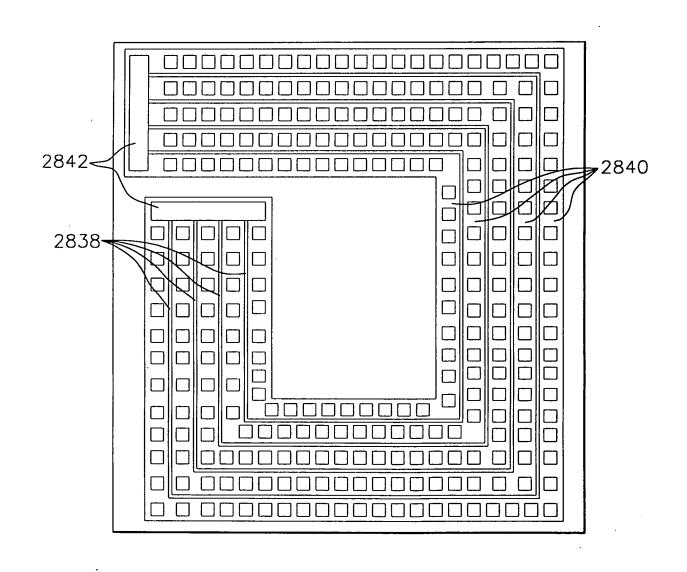


FIG.28j

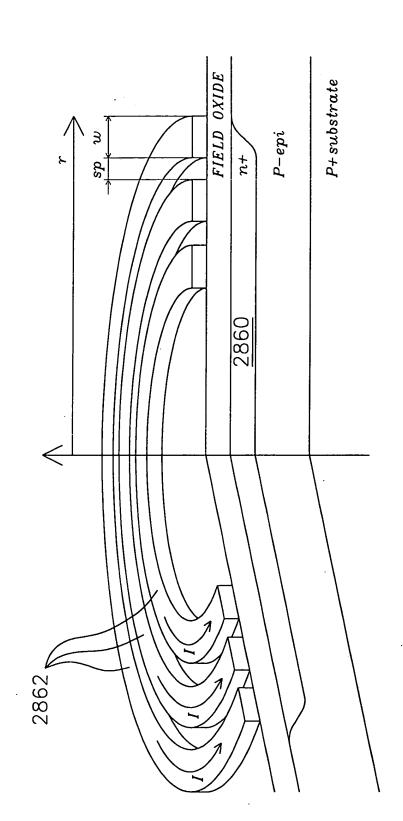


FIG.28k

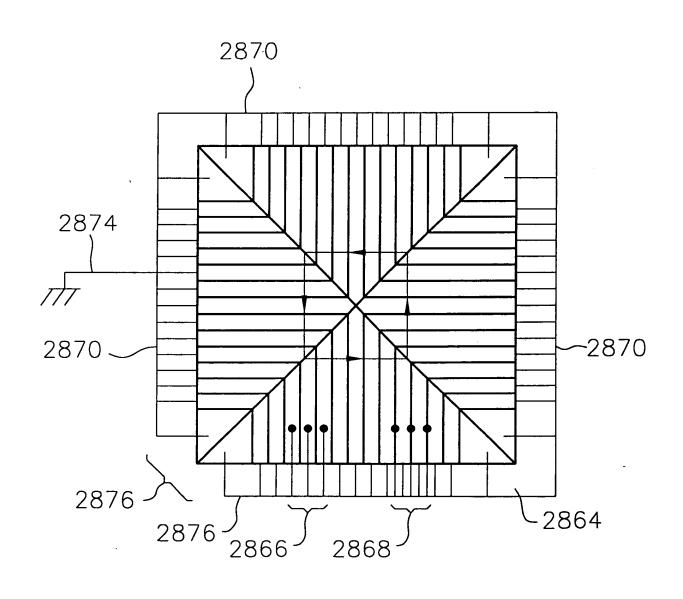
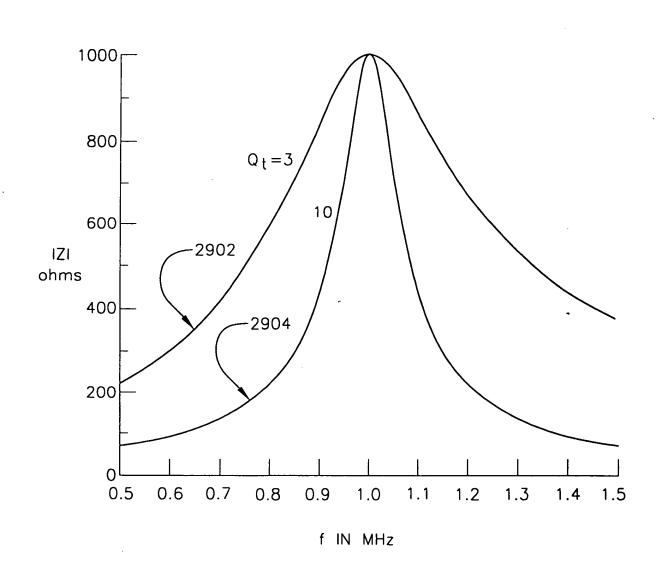
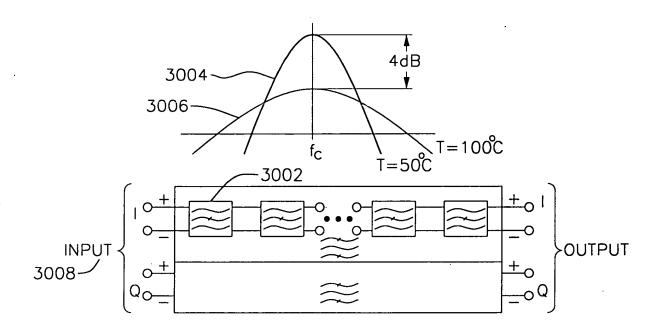


FIG.29







 $FIG.31\alpha$ 

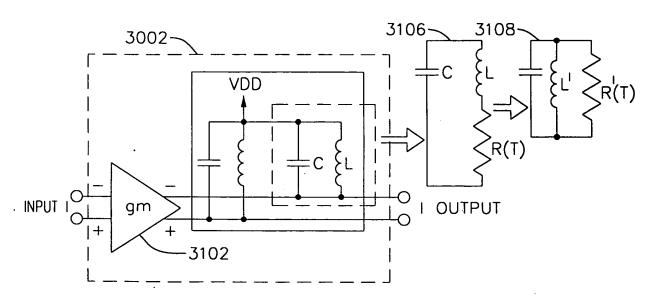


FIG.31b

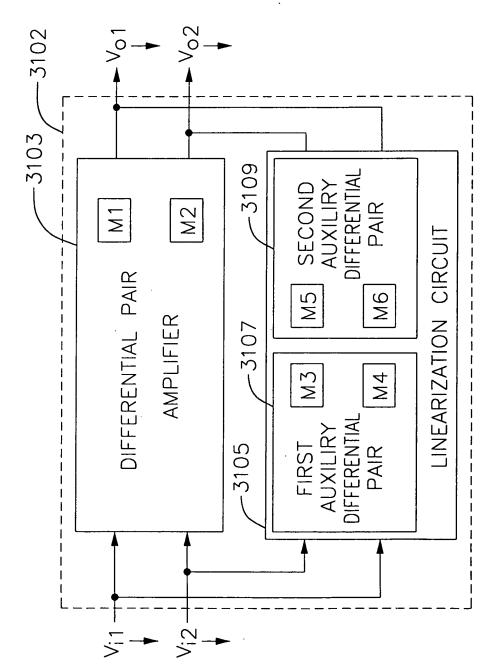
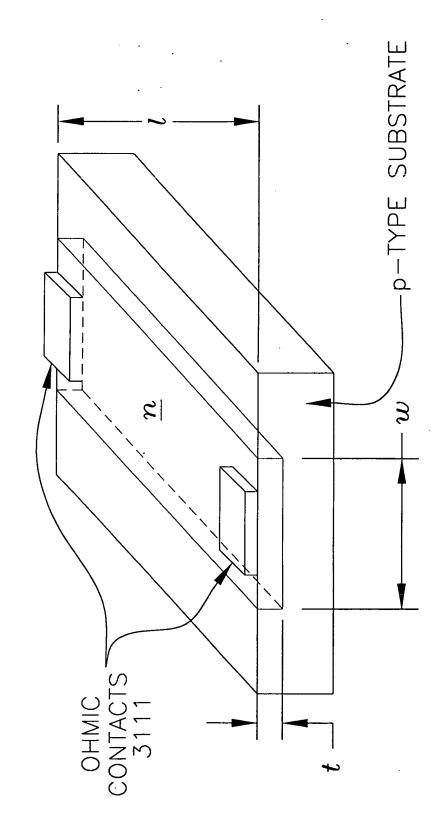


FIG.31c



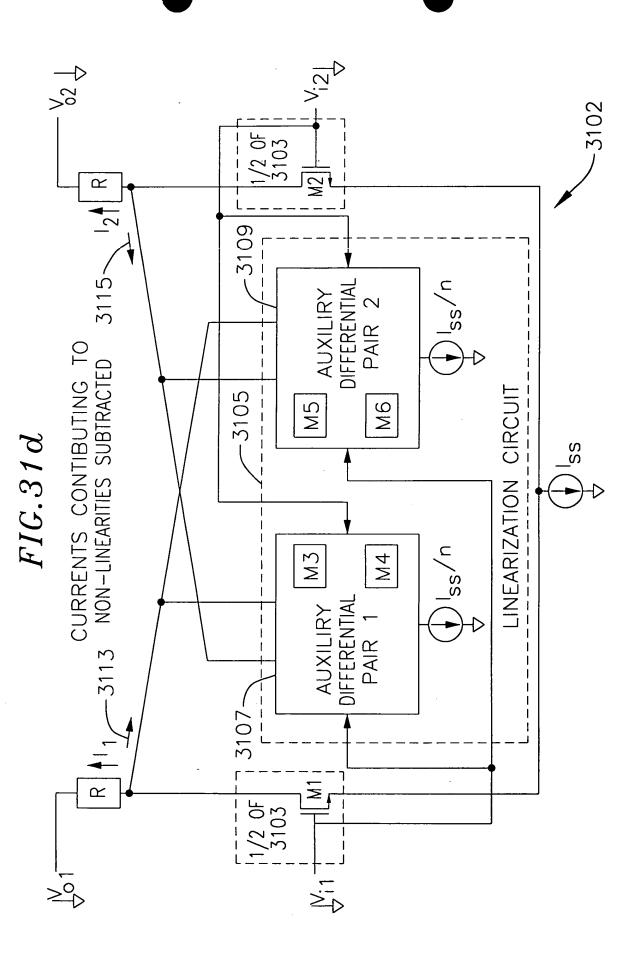


FIG.31e

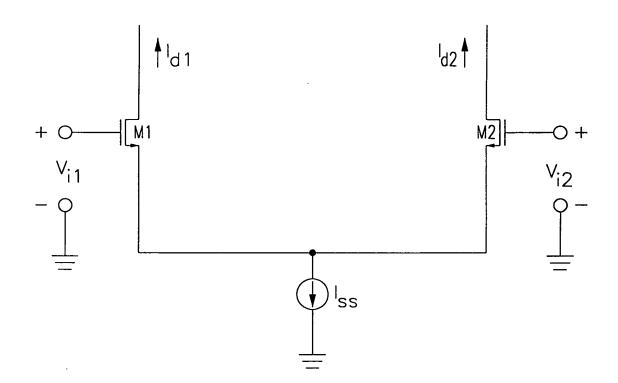
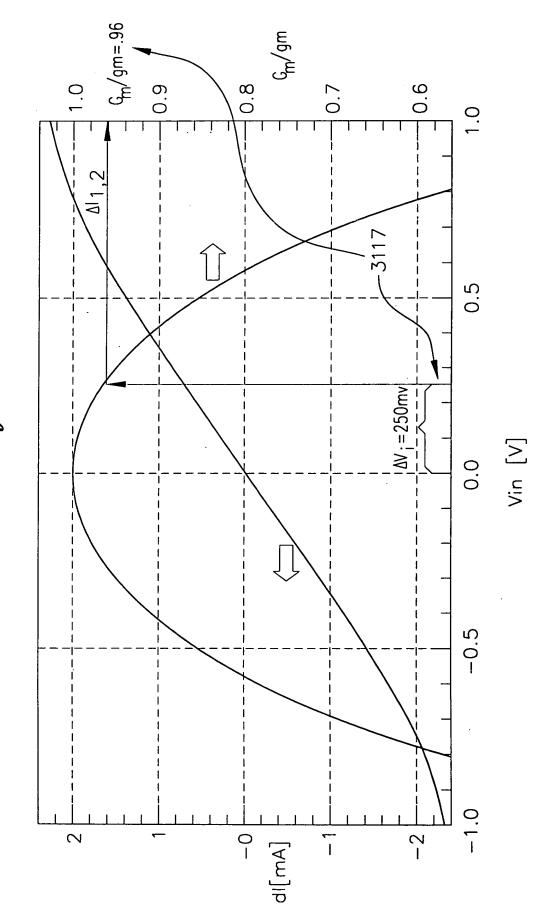


FIG.31f



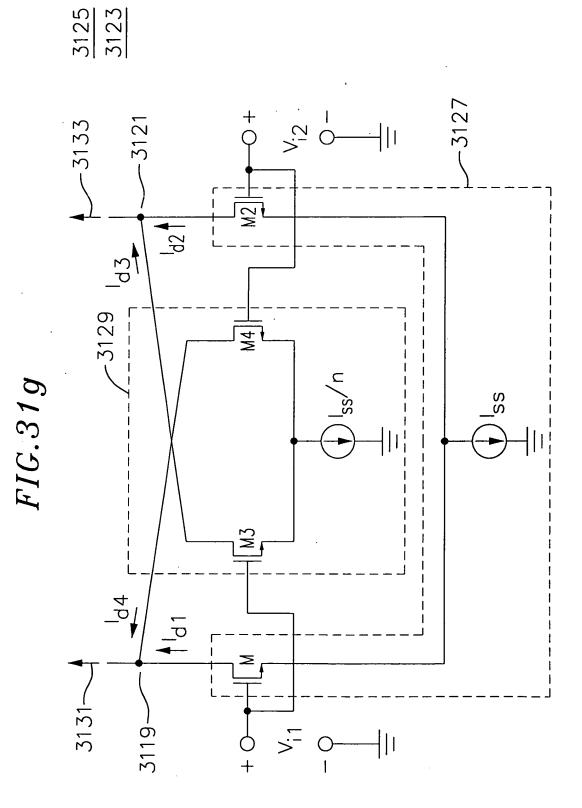
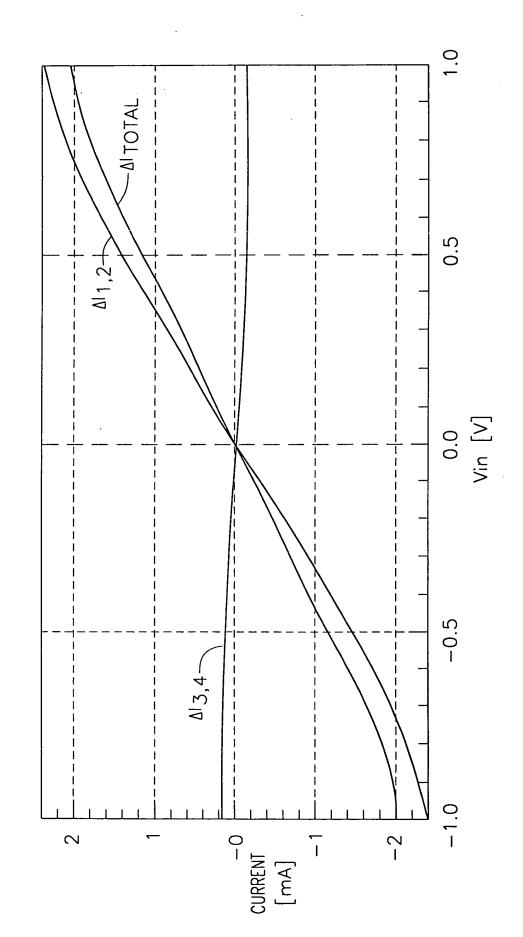
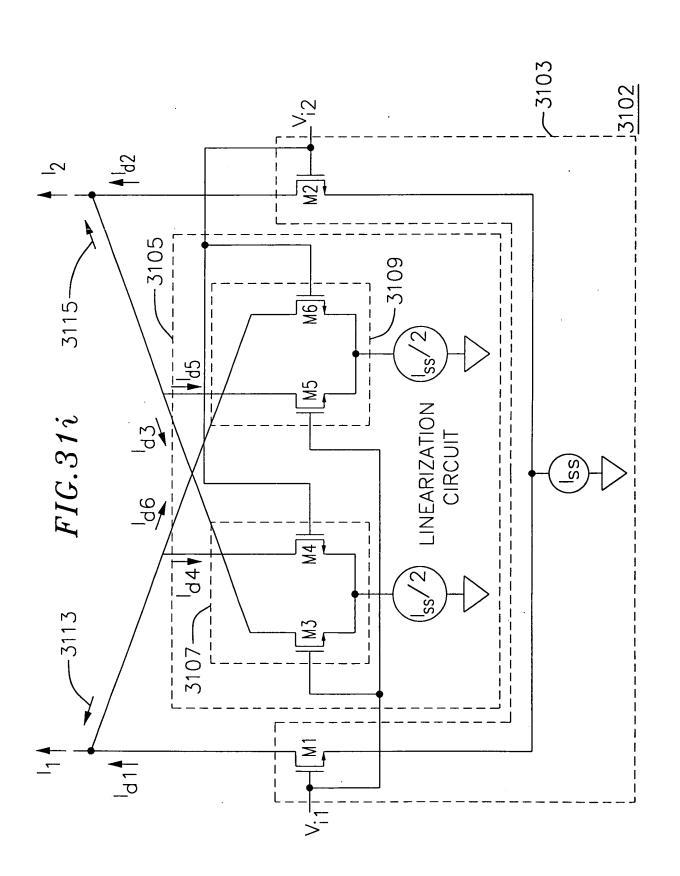


FIG.31h

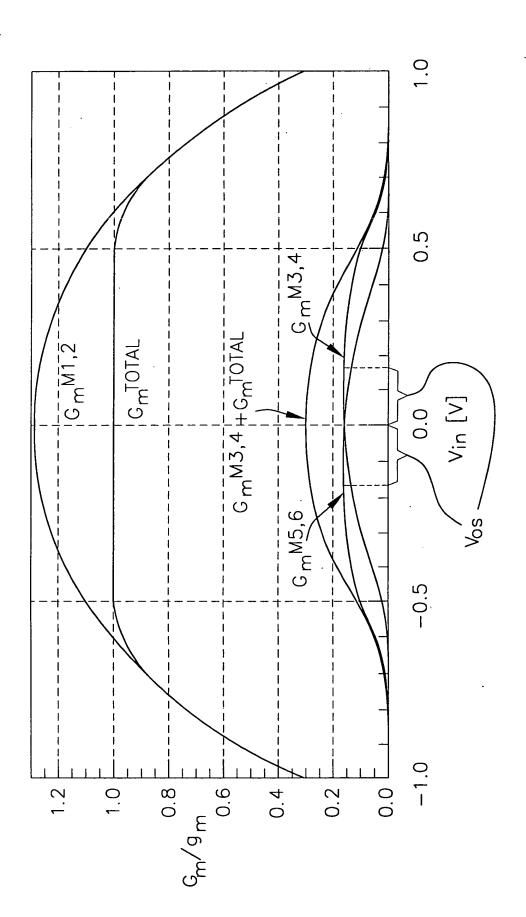




-VITOTAL 0.5 -3135 FIG.31j 0.0 Vin [V] 13,4-N5,6--0.5\_O CURRENT [mA] ~ -2

ndyadrio laison

FIG.31k



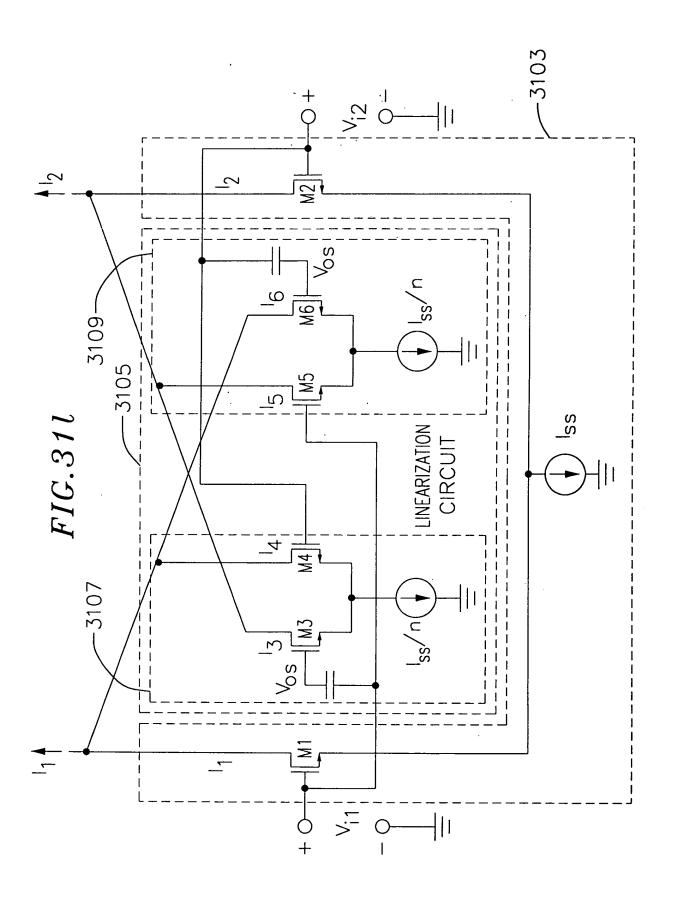
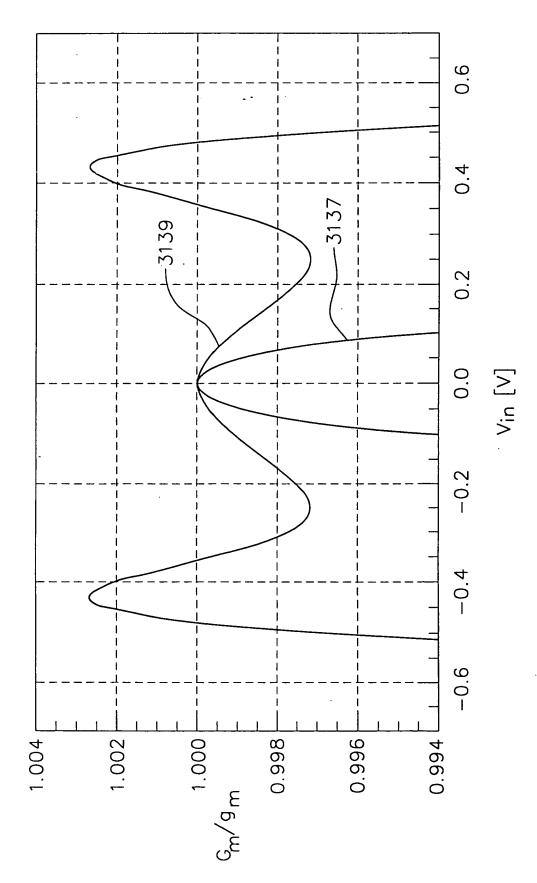


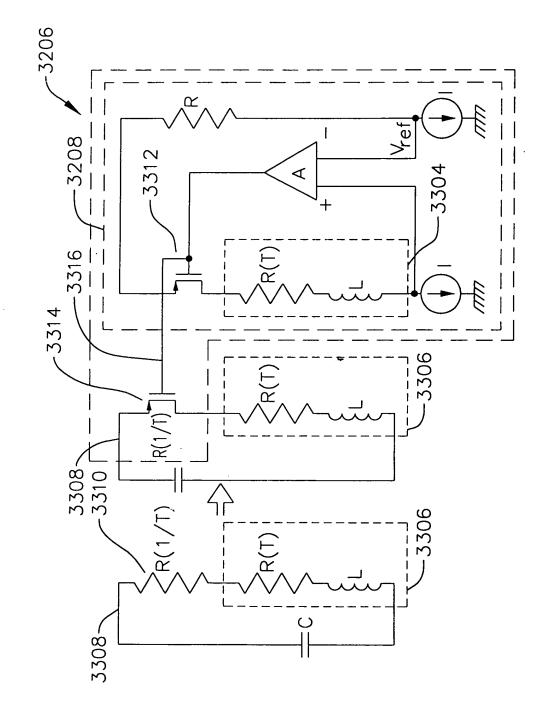
FIG.31m



 $\left\langle -R(T) = \right\rangle$ -3204 -OUTPUT -3206 -3208 000+ -3002 3314 CONTROL -3306 -3208 Ся day : CONTROL 3202-110 3306--3102 3206~ 3104-3314 g + +100 INPUT.

FIG.32

FIG.33



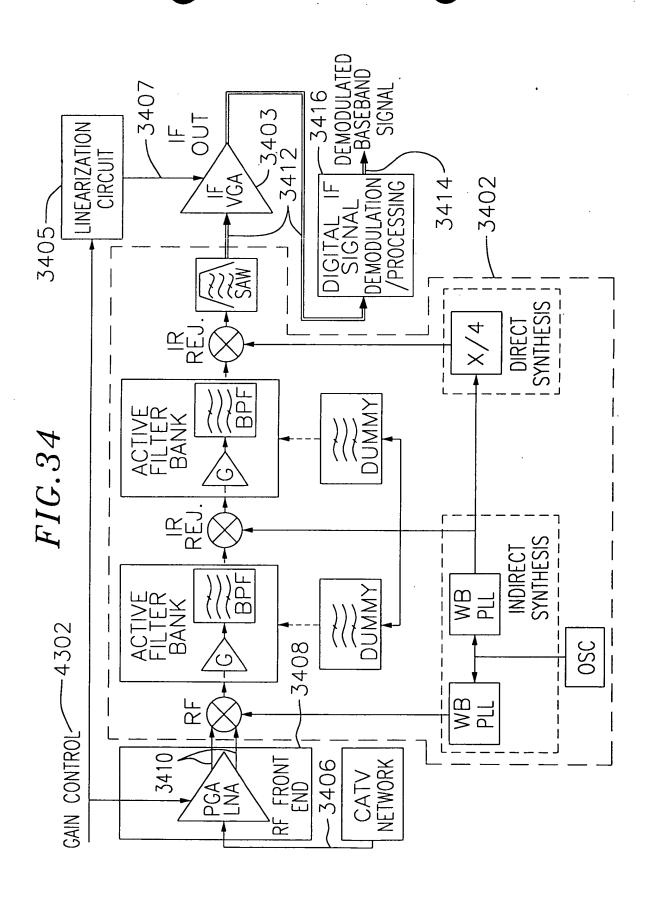
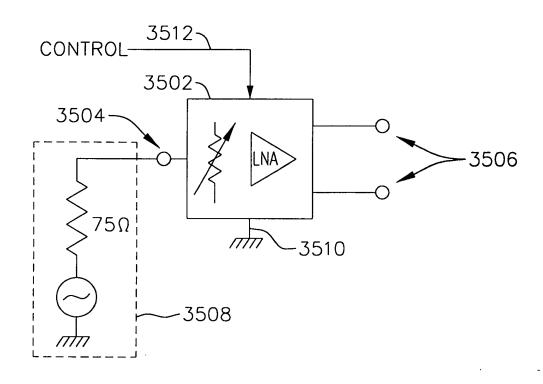
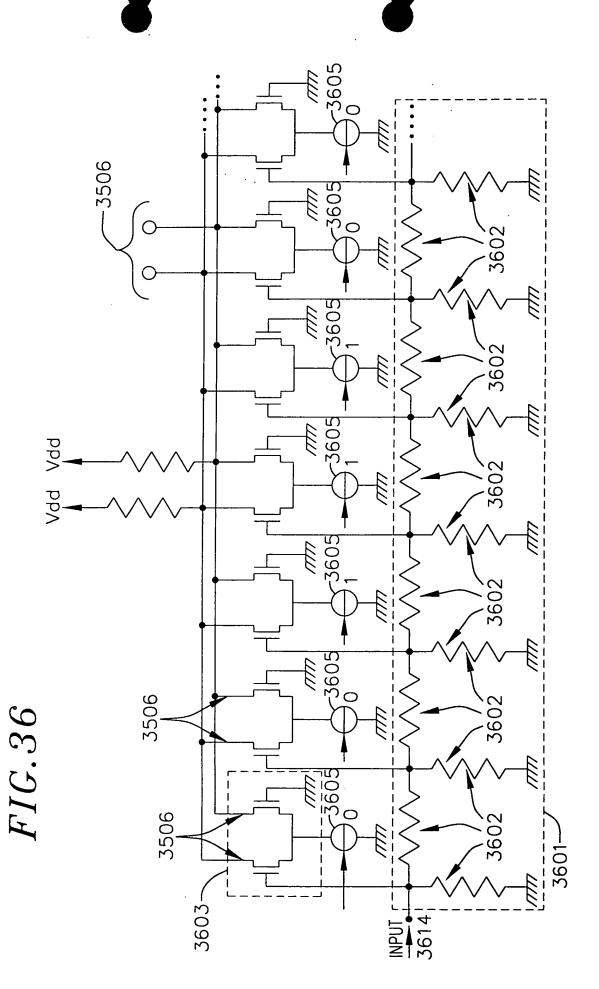
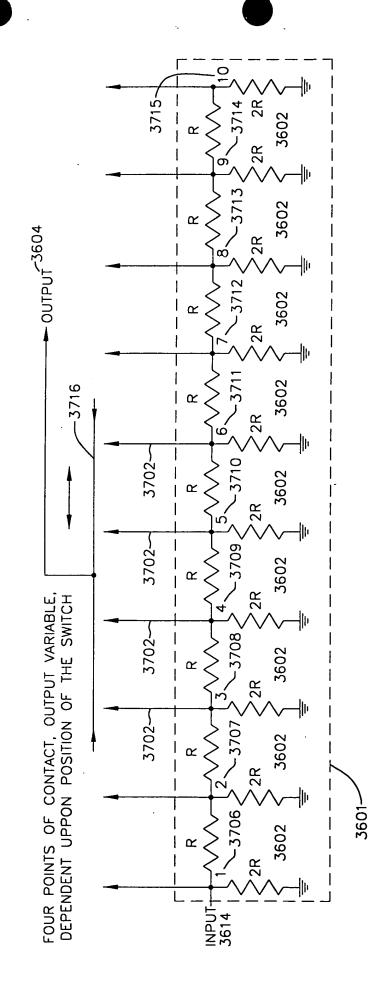


FIG.35





## FIG.37

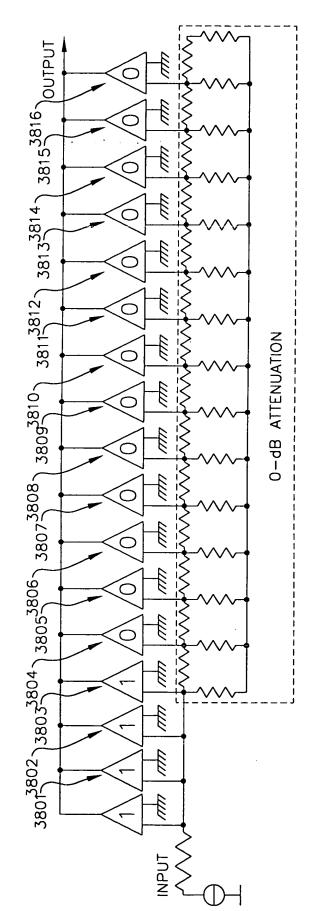


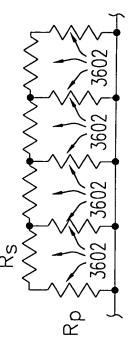
8



FIG.38

PGA SETTINGS





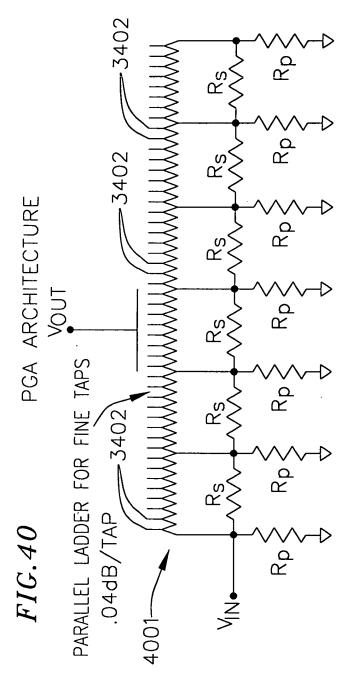


FIG. 41

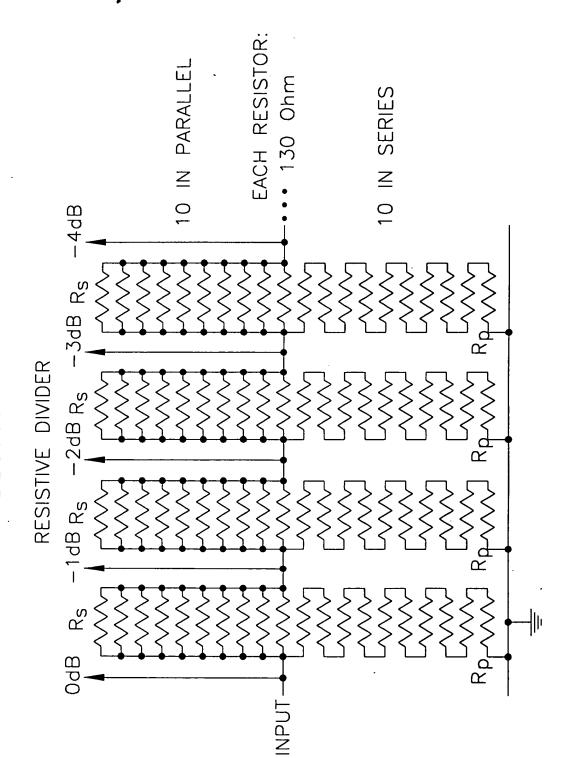
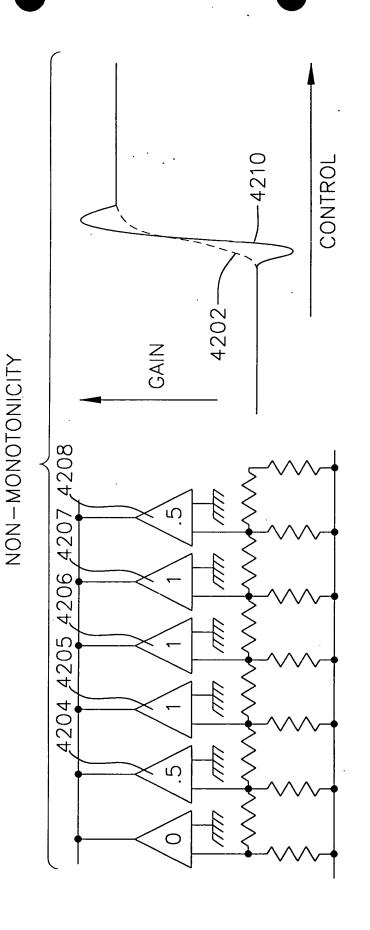
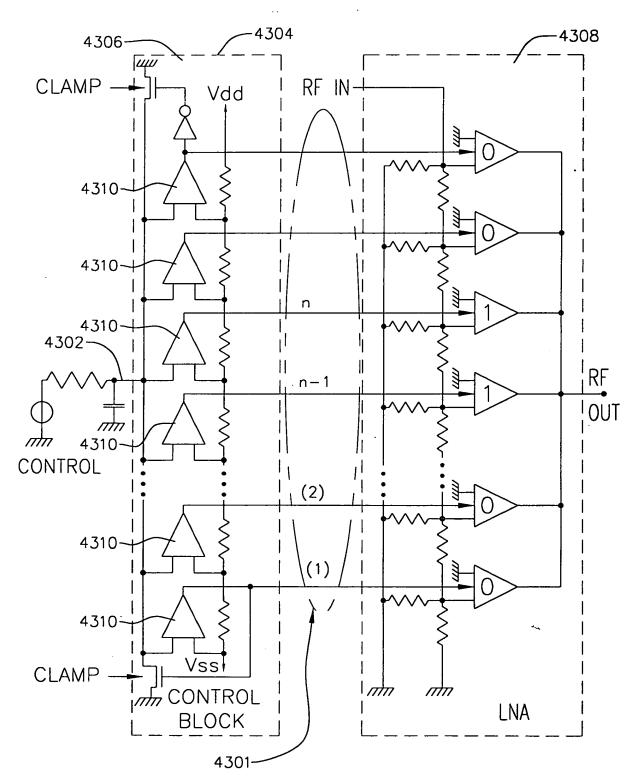
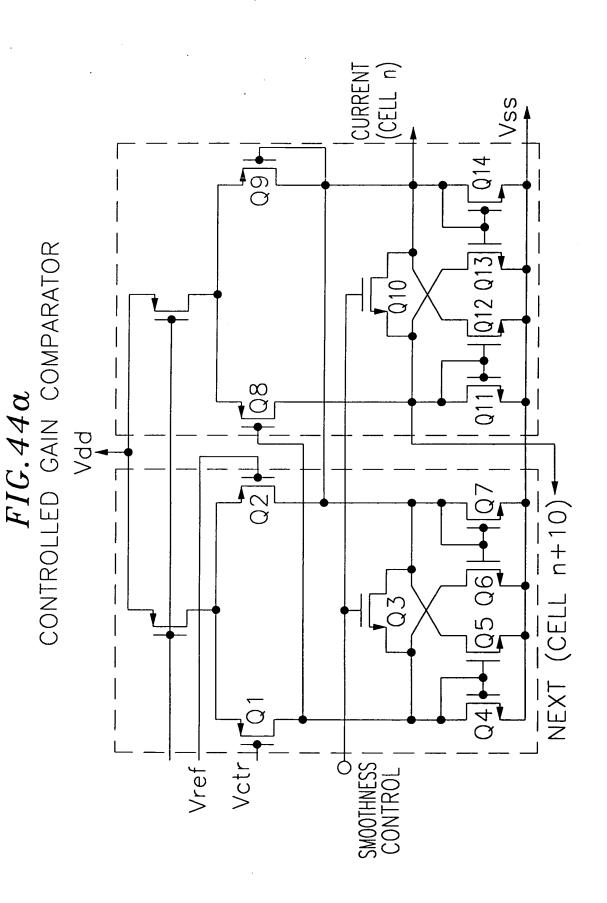


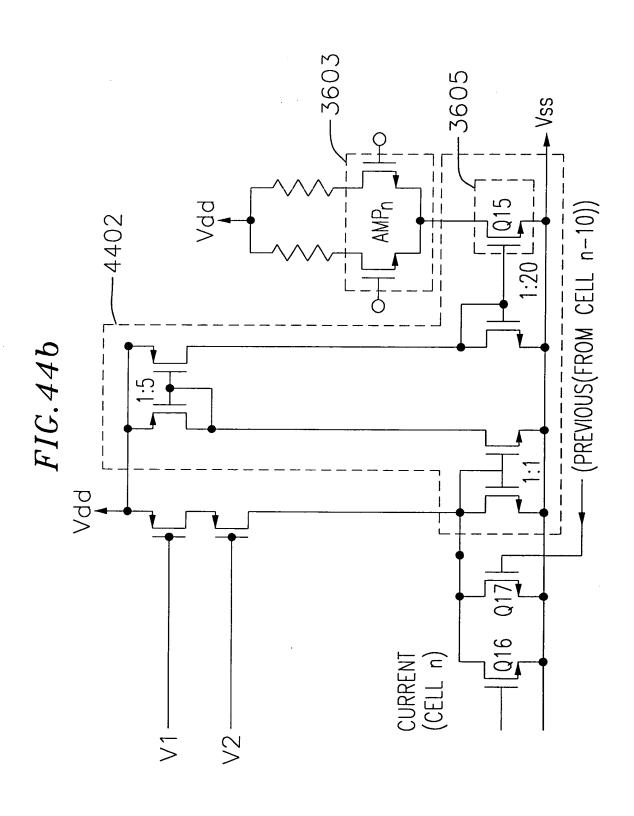
FIG.42











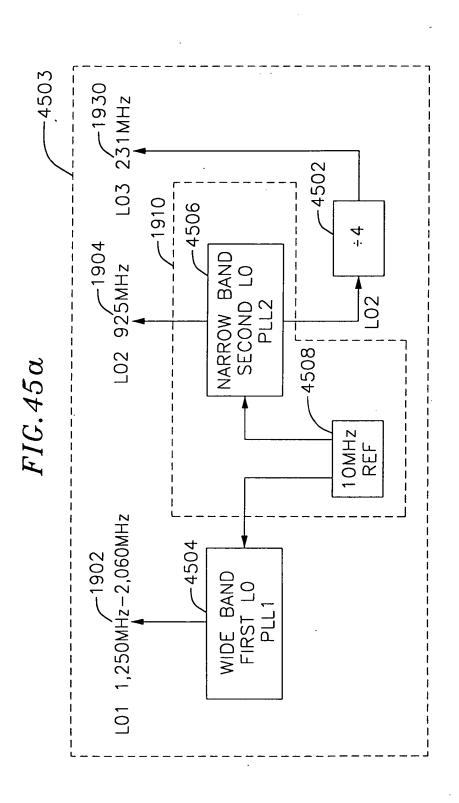
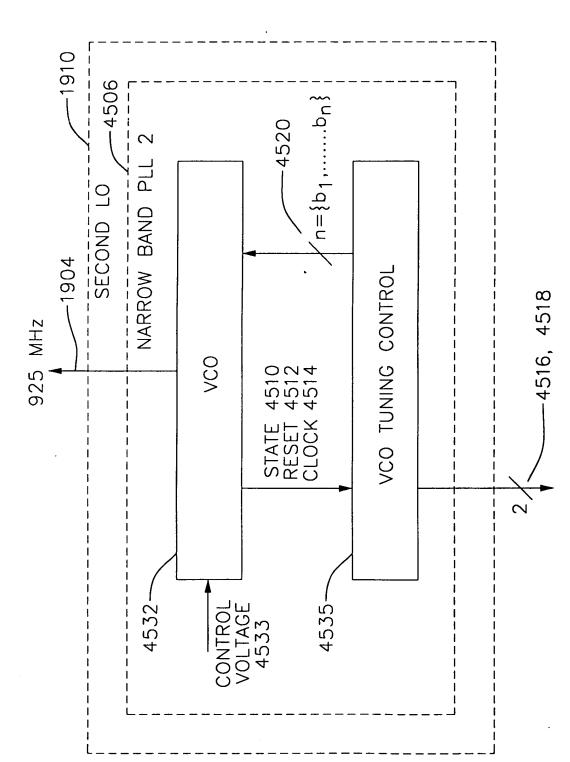
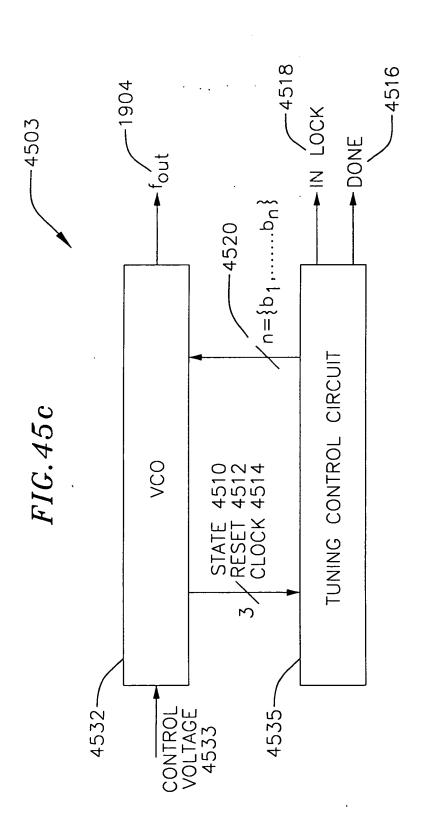
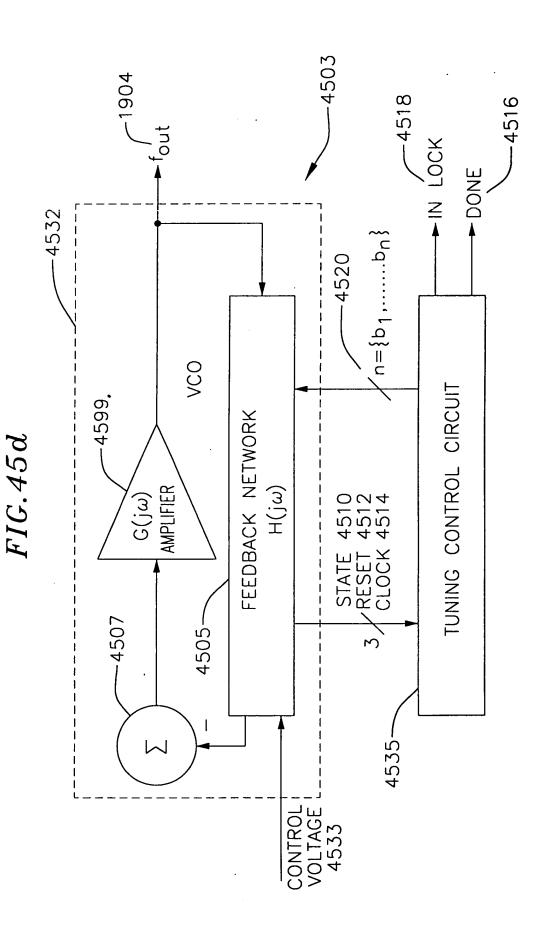


FIG. 45b







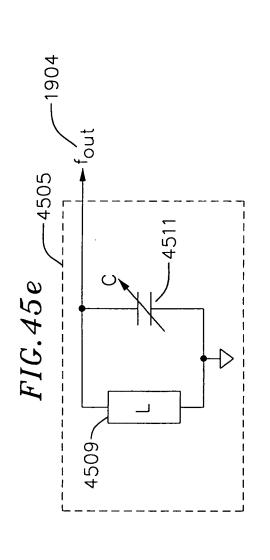


FIG.45f

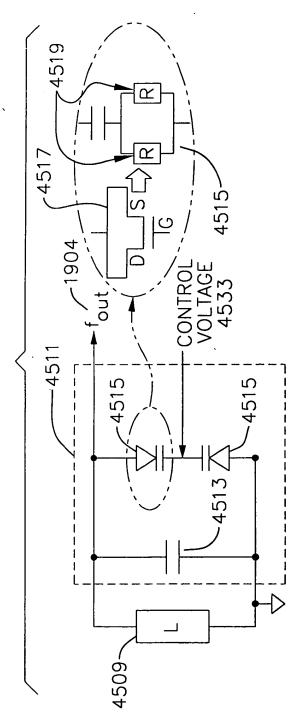
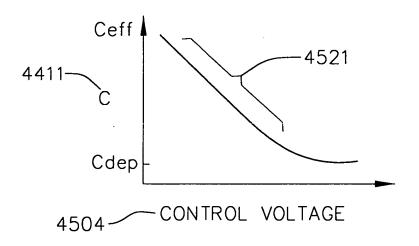
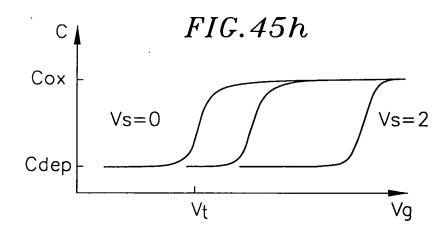
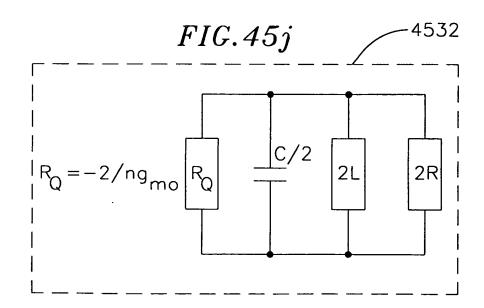


FIG.45g capacitance vs control voltage







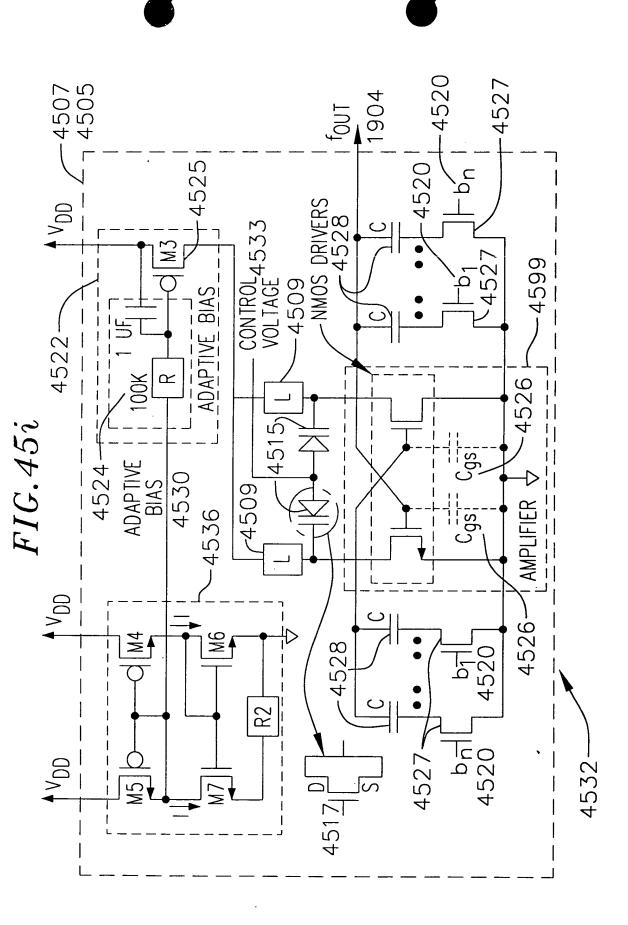
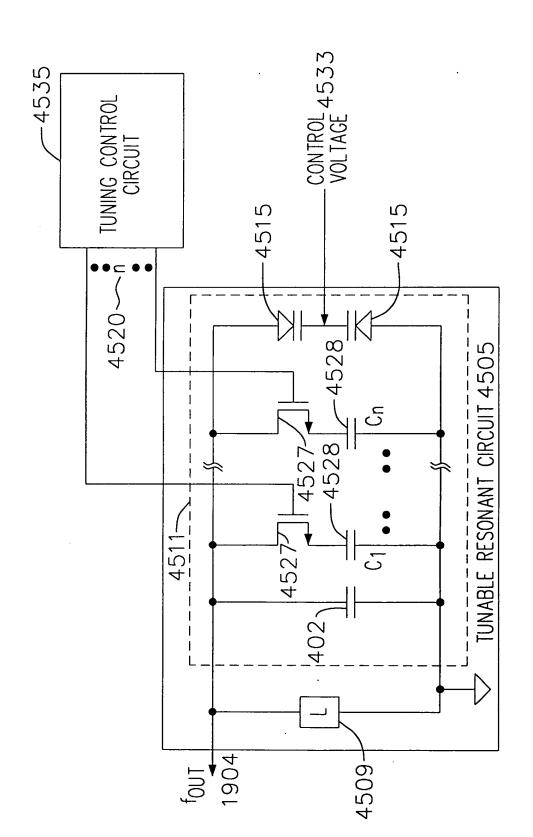


FIG. 45k



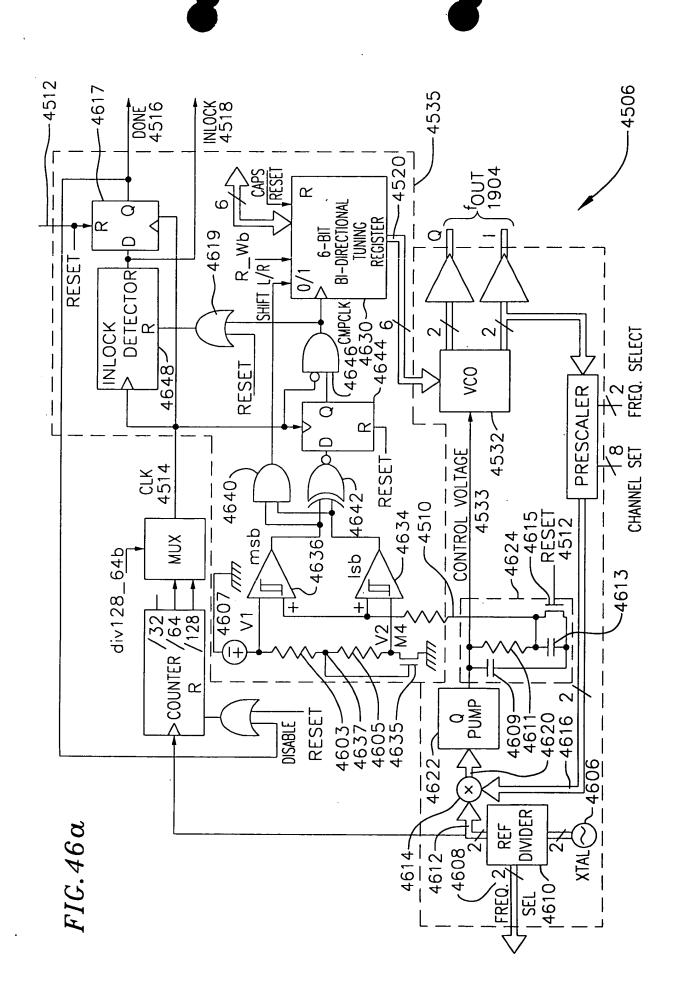
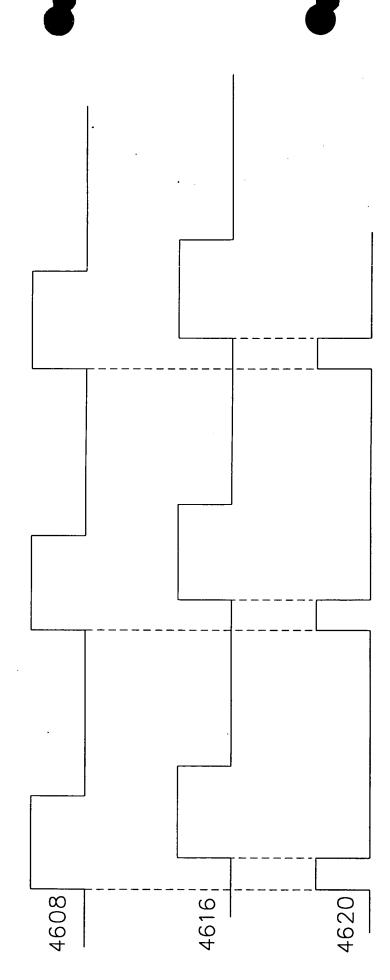


FIG.46b



 $FIG.47\alpha$ 

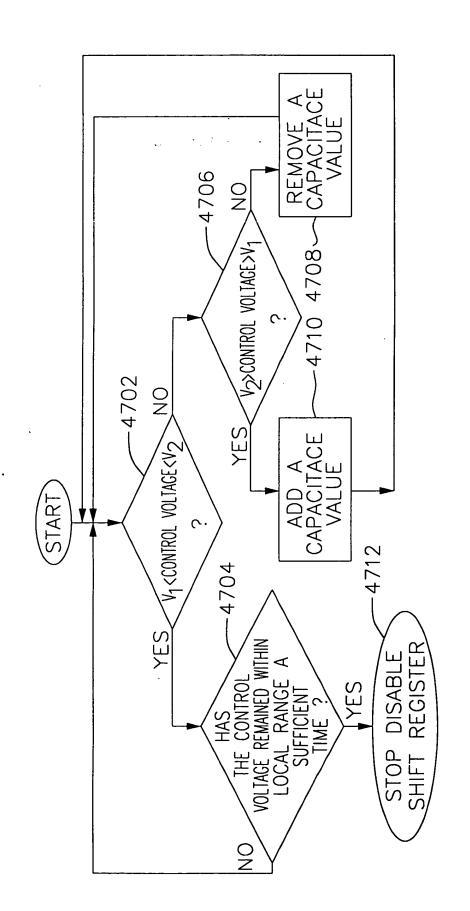
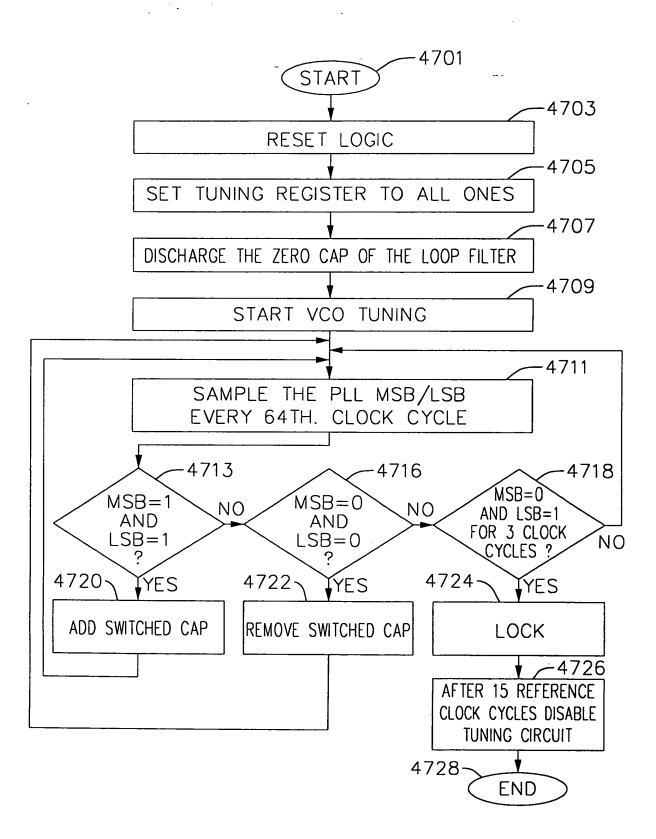
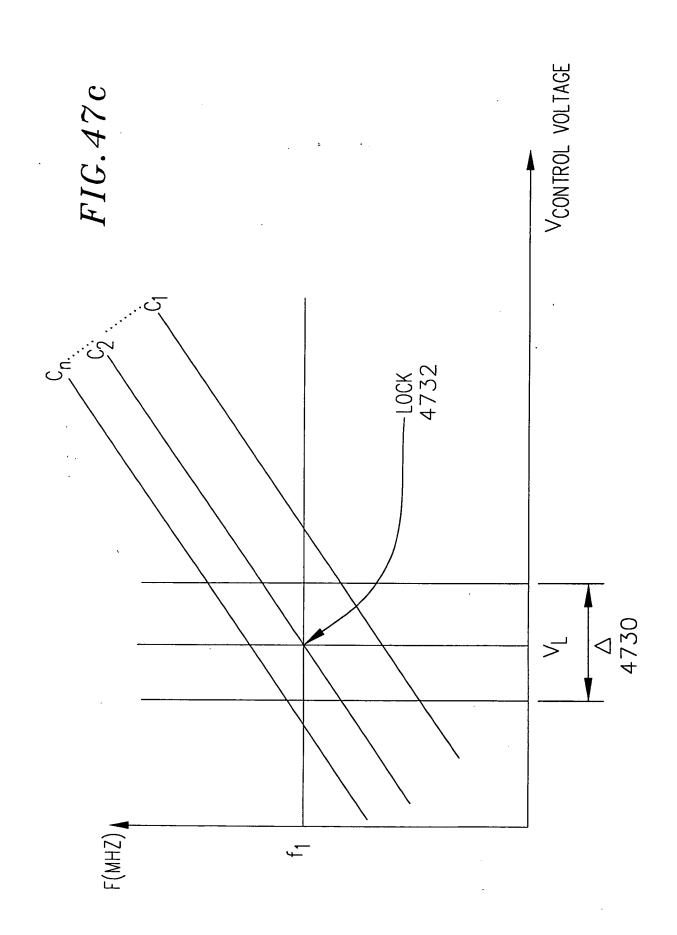


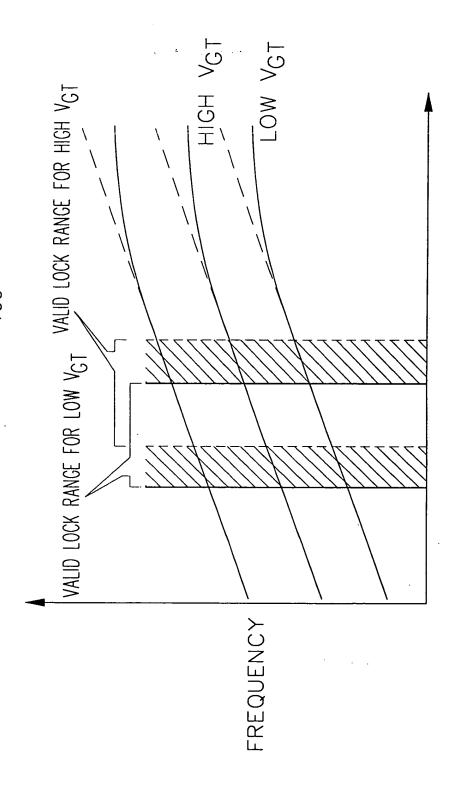
FIG. 47b



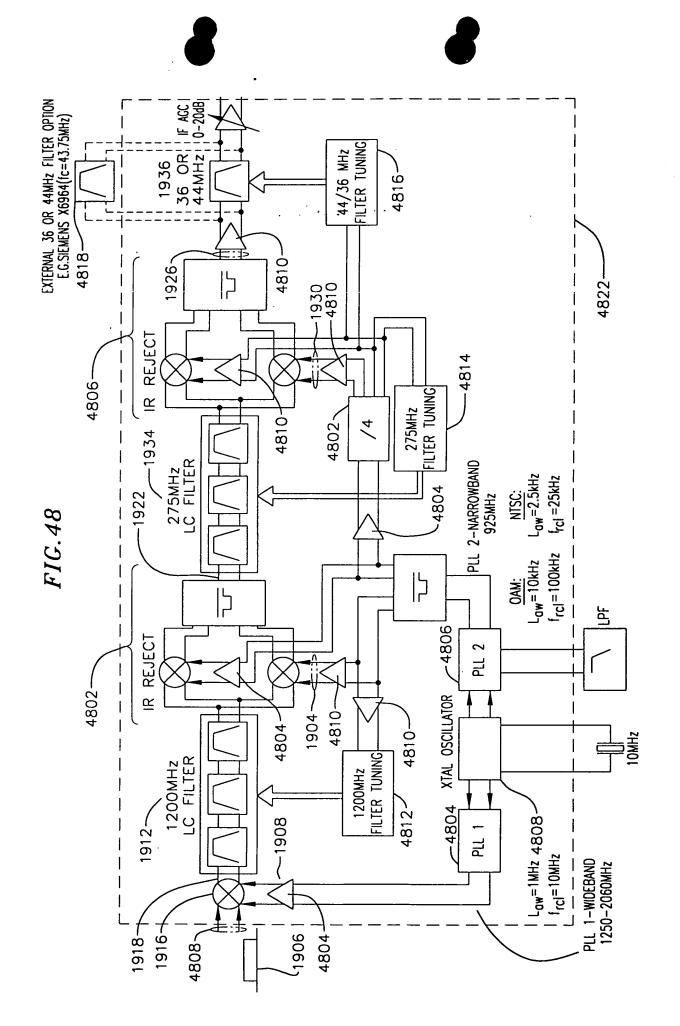


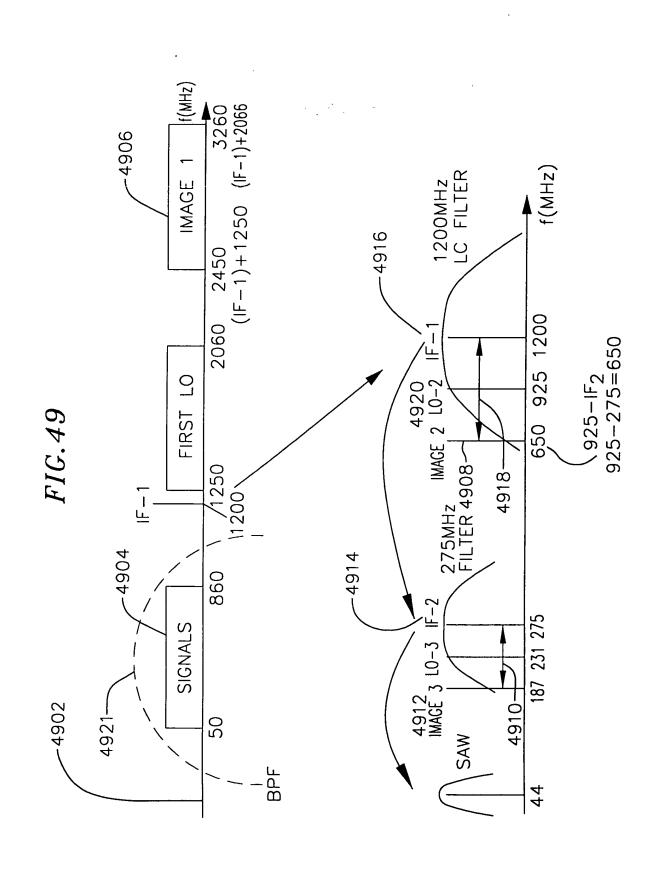
## FIG. 47d

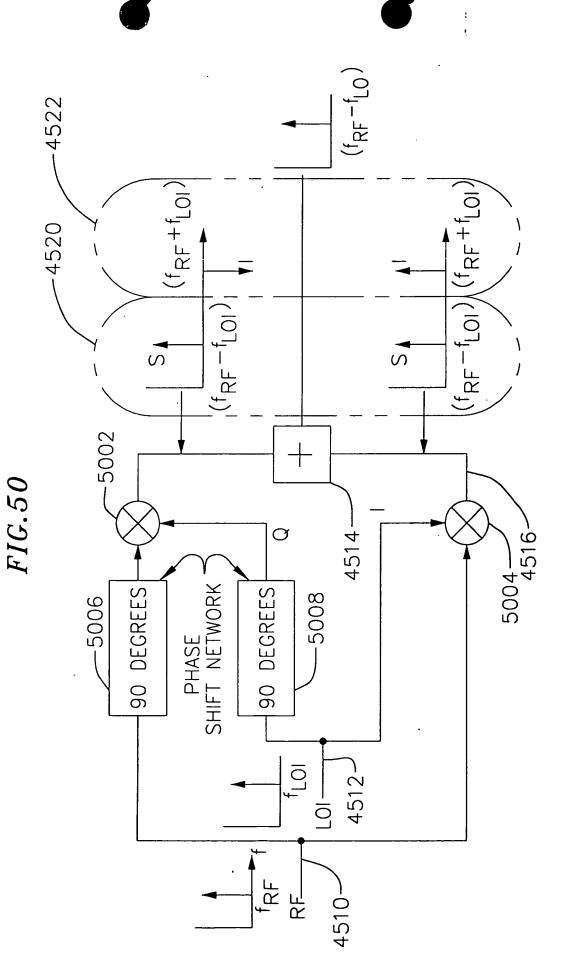
REPRESENTATIVE K<sub>VCO</sub> CURVES

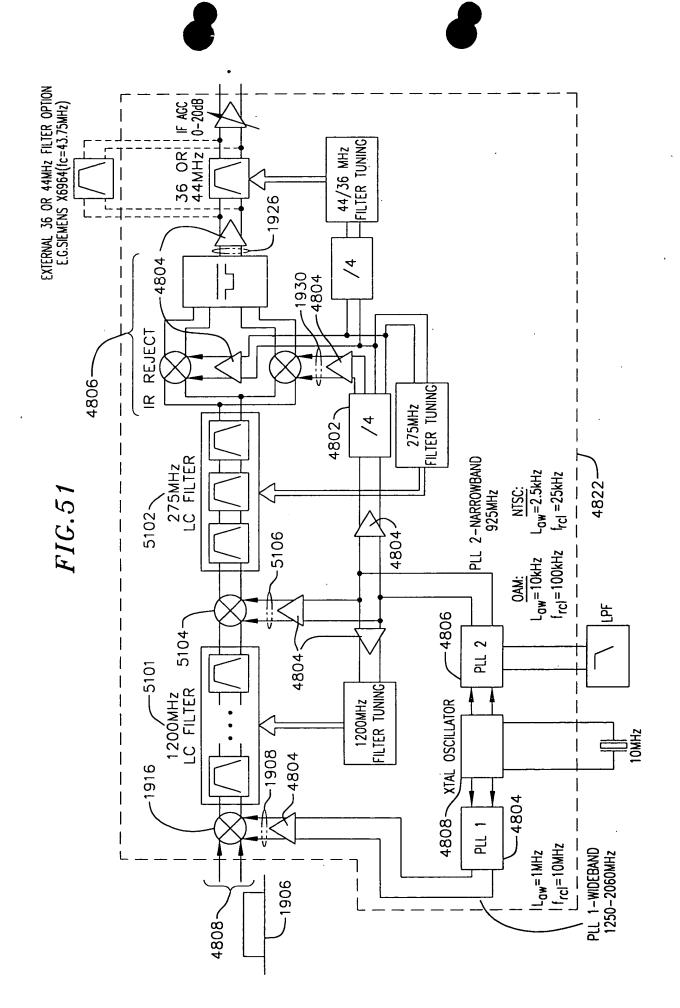


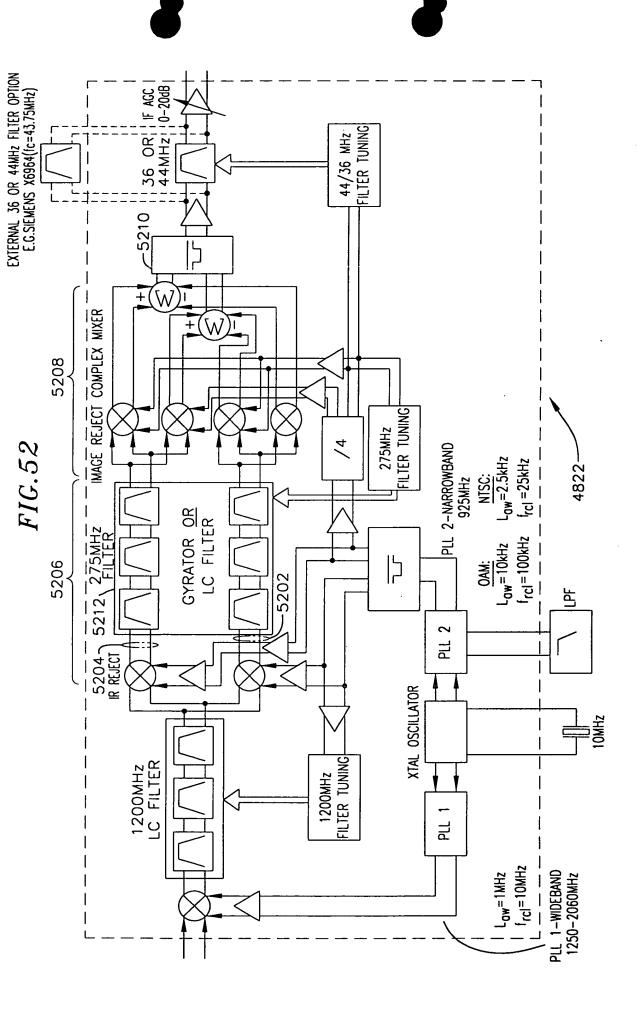
CONTROL VOLTAGE







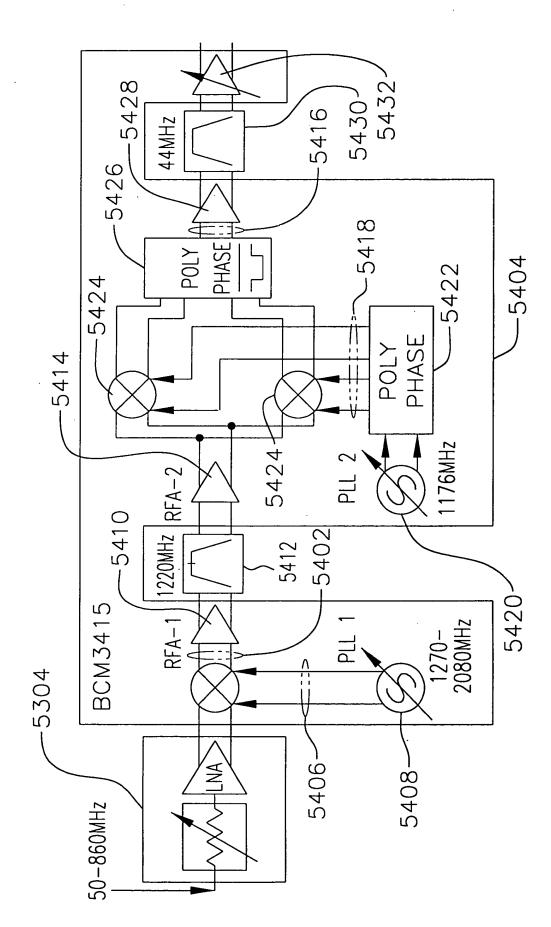


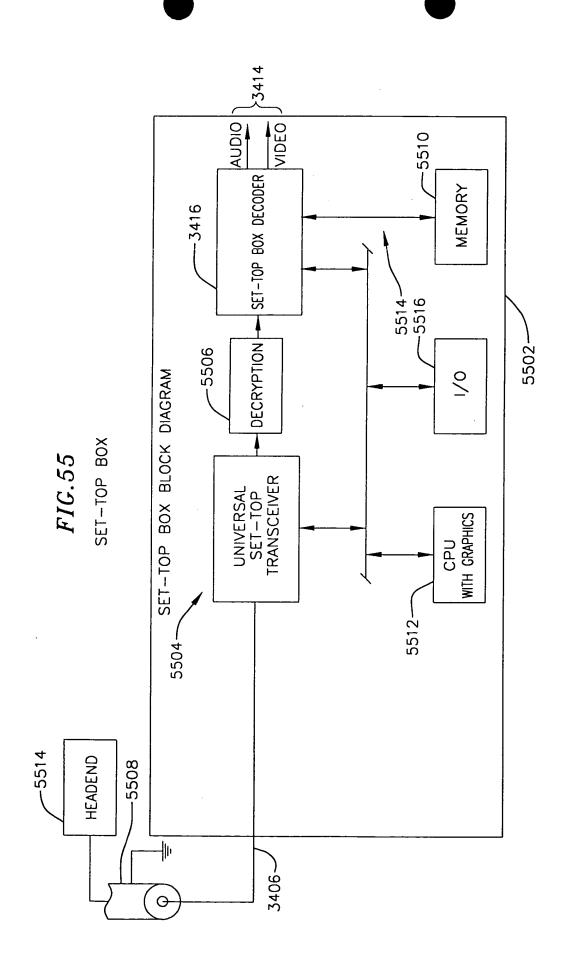


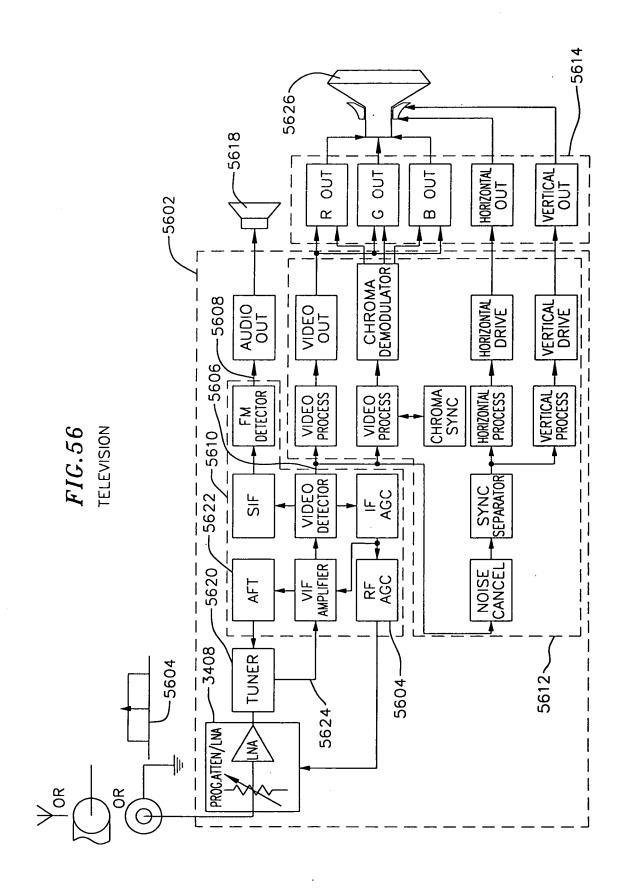
IF ACC 0-20dB 36 OR 44MHz IR REJECT 275MHz FILTER TUNING 4 / PLL 2-NARROWBAND 925MHz  $\frac{\text{NTSC}}{L_{QW}=2.5\text{kHz}}$ frel =25kHz 275MHz LC FILTER OAM: L<sub>aw</sub>=10kHz f<sub>rcl</sub>=100kHz CATV TUNER FIG.53| | (%) || P. PLL 2 IR REJECT XTAL OSCILLATOR 10MHz 1200MHz FILTER TUNING 1200MHz LC FILTER | L<sub>ow</sub>=1MHz 5302 면 1 PLL 1-WIDEBAND | 1250-2060MHz | -5304 RF AGC

( | 1 | 1

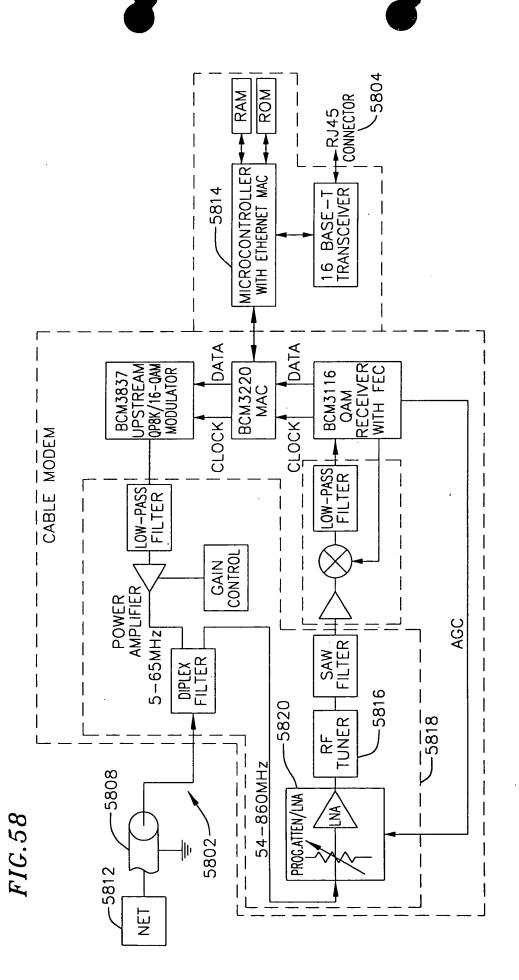
FIG.54

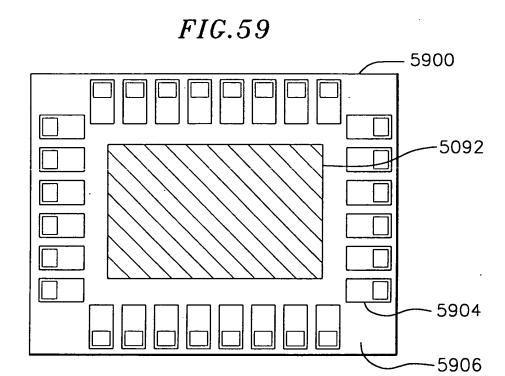






MODULATOR F OUT VIDEO OUTPUT 5706 SIGNAL SWITCH UNIT RECORDING UNIT 00.7  $\infty$ -5708 TAPE ⋖  $\underline{Z}$ 5710-FIG.57VCR BLOCK DIAGRAM SIGNAL VIDEO SIGNAL **PROCESSOR PROCESSOR** AUDIO CONTROLLER RECORDING AUDIO SYNC OR AGC DETECTOR VIDEO ΖC TAPE LNU PROCESSOR ON-SCREEN DISPLAY VIF AND SIF AMPLIFIERS AND DETECTORS 5708-RECEIVER **KEYBOARD** EEPROM LOCAL <u>«</u> -5702 CONTROL CONTROL ASSEMBLY BAND TUNER TIMER ROM RAM CPU -5704





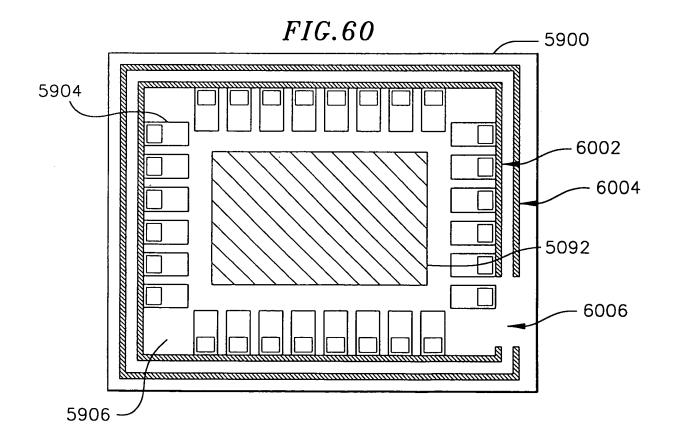


FIG. 61

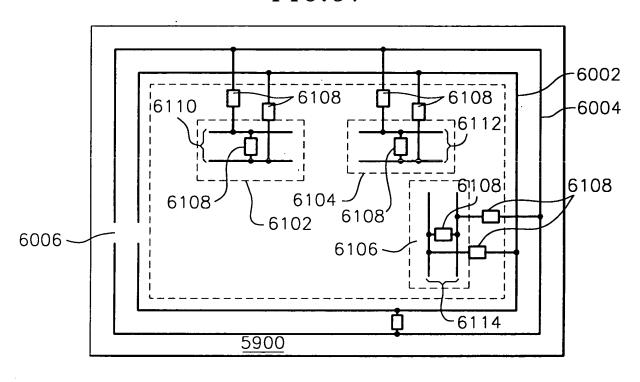


FIG. 62

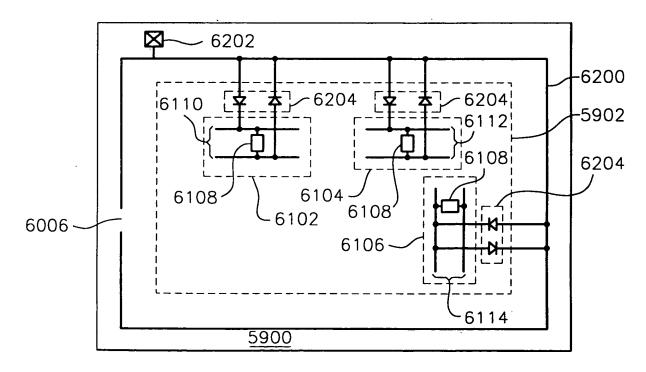


FIG.63

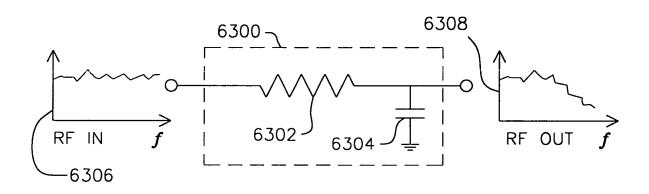


FIG. 64

FIG. 65

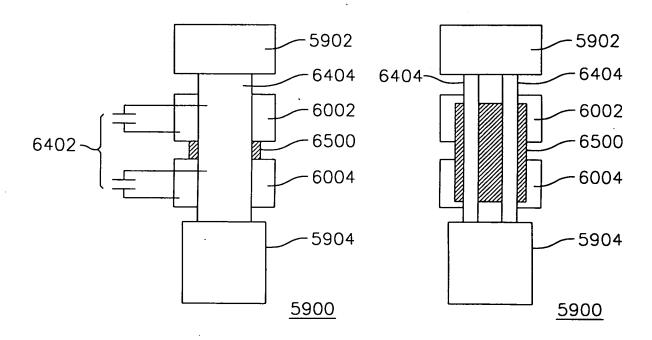


FIG. 66

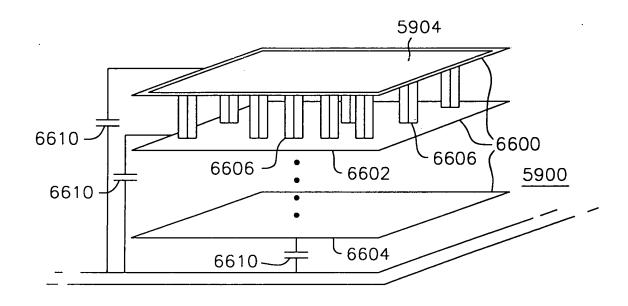


FIG.67

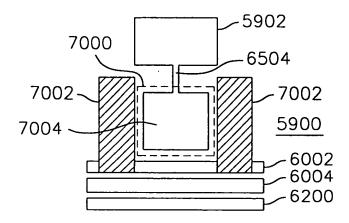
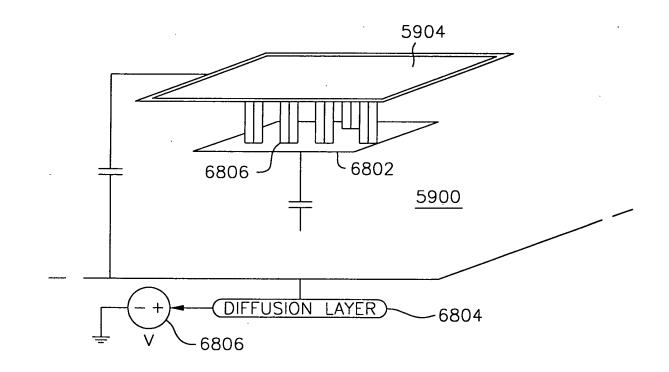
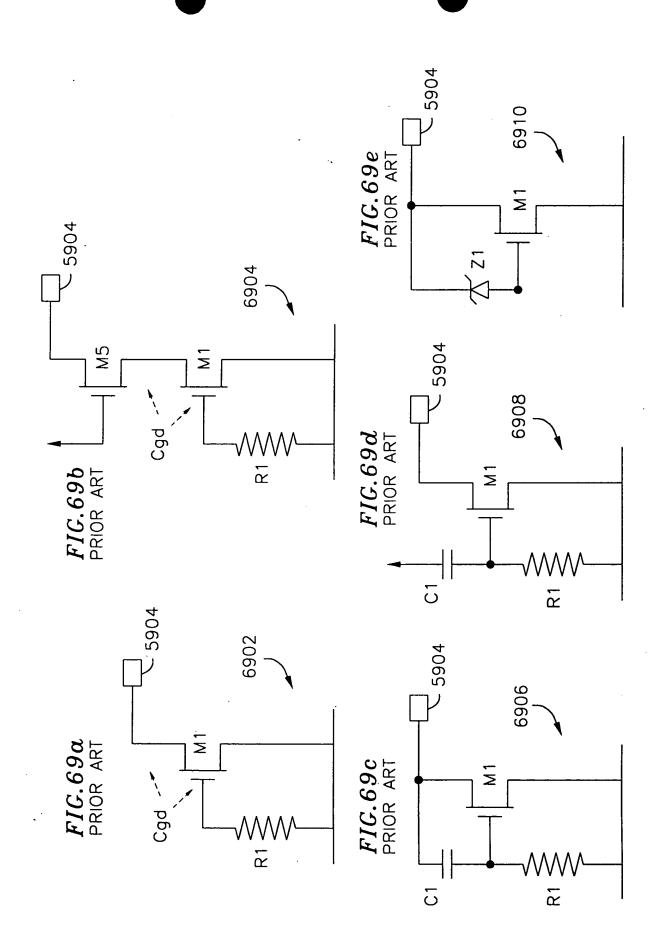
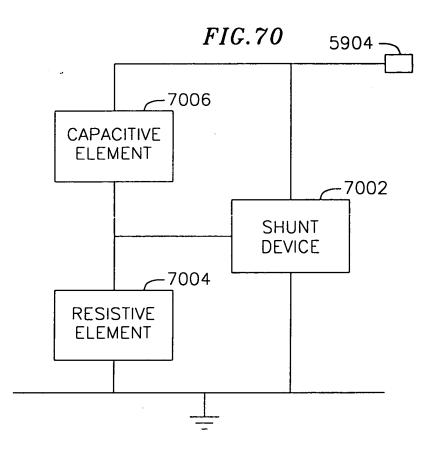
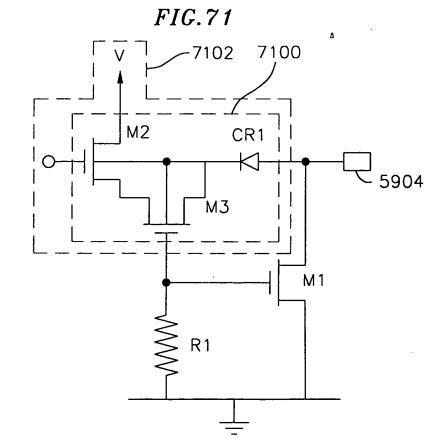


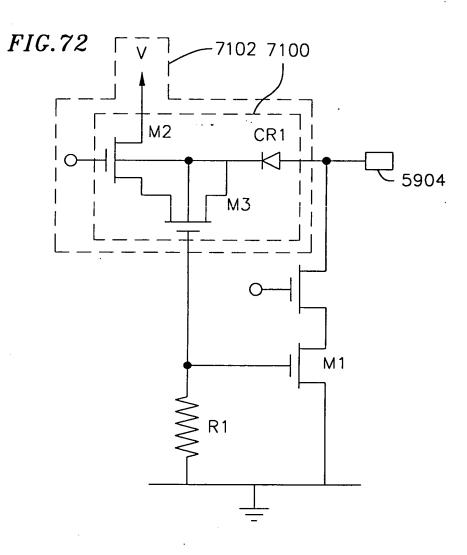
FIG. 68











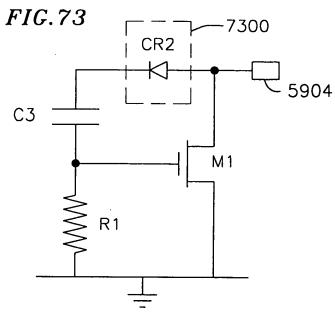
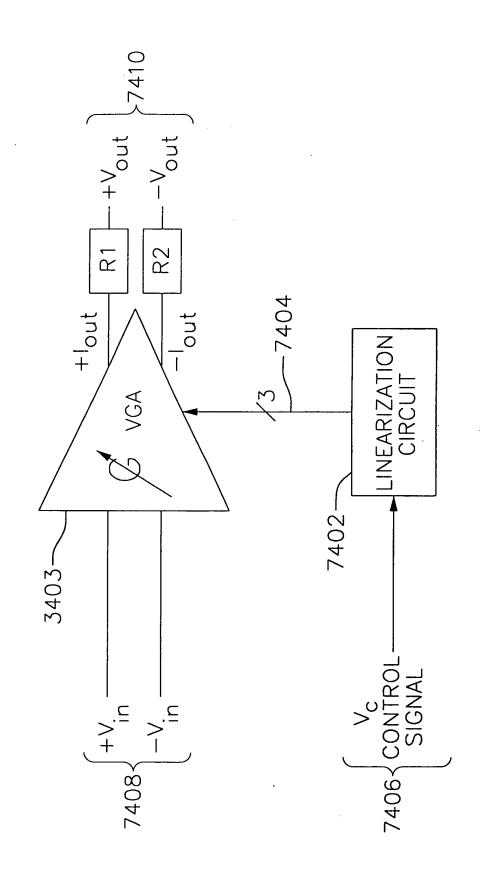


FIG. 74



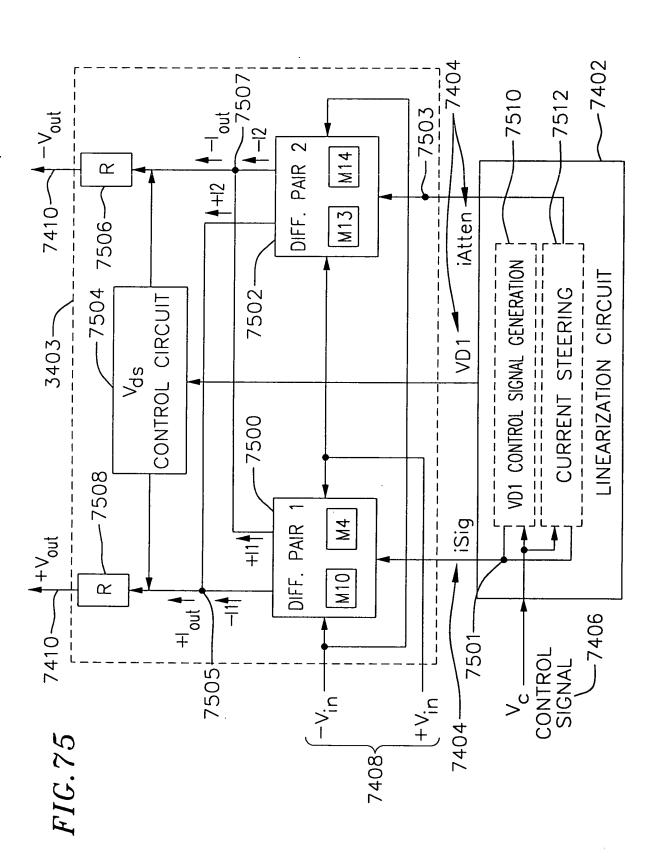
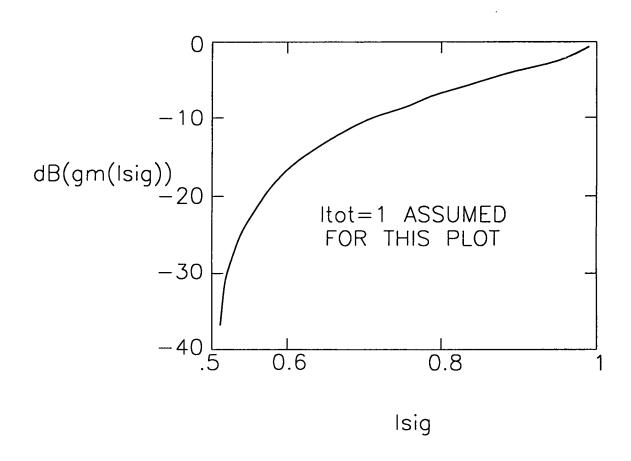


FIG. 76



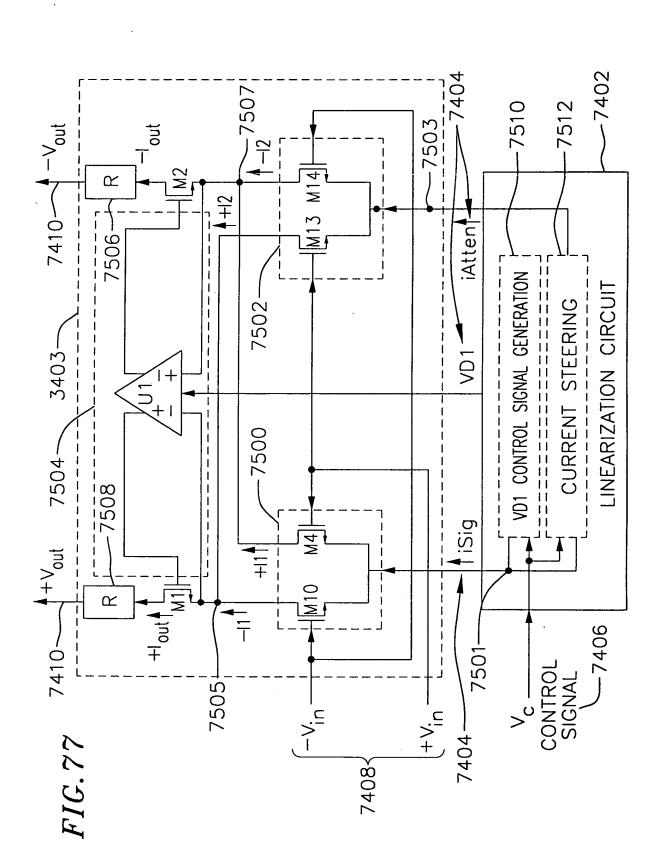


FIG. 78b

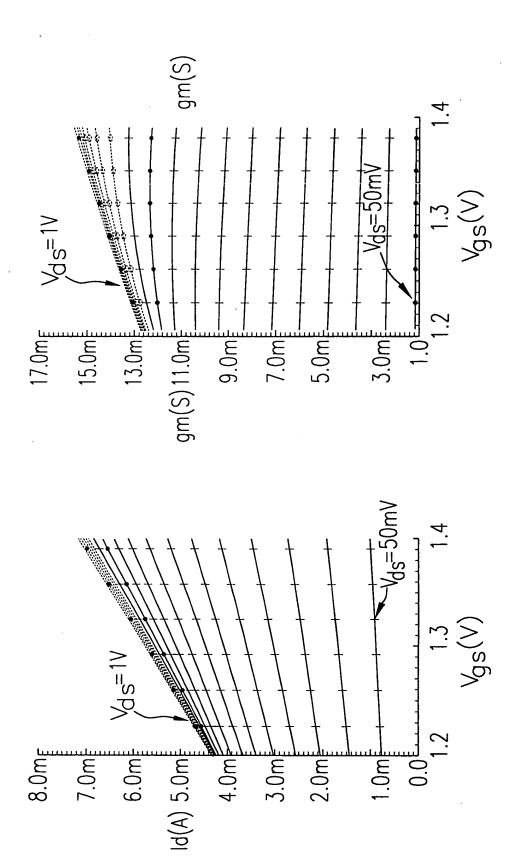
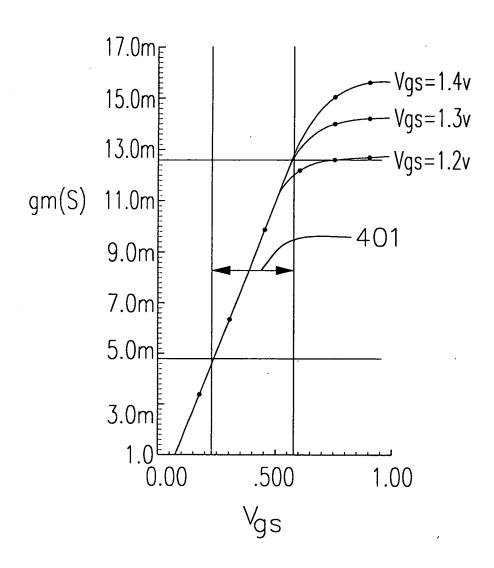
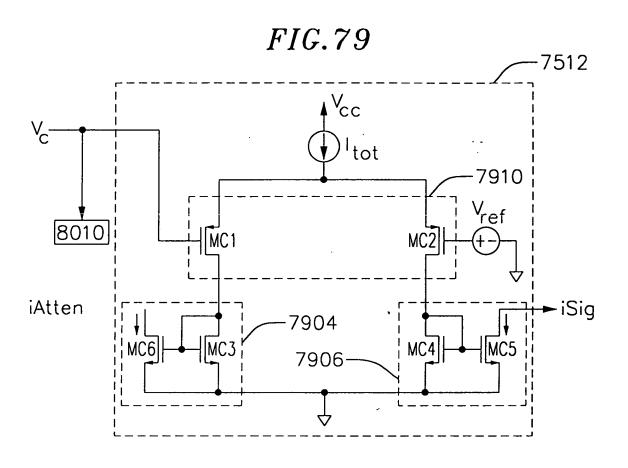
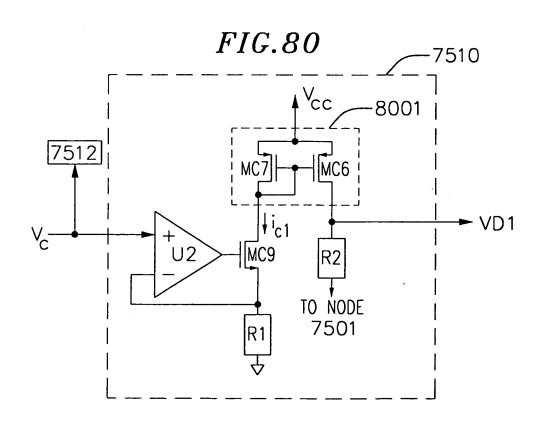


FIG. 78c







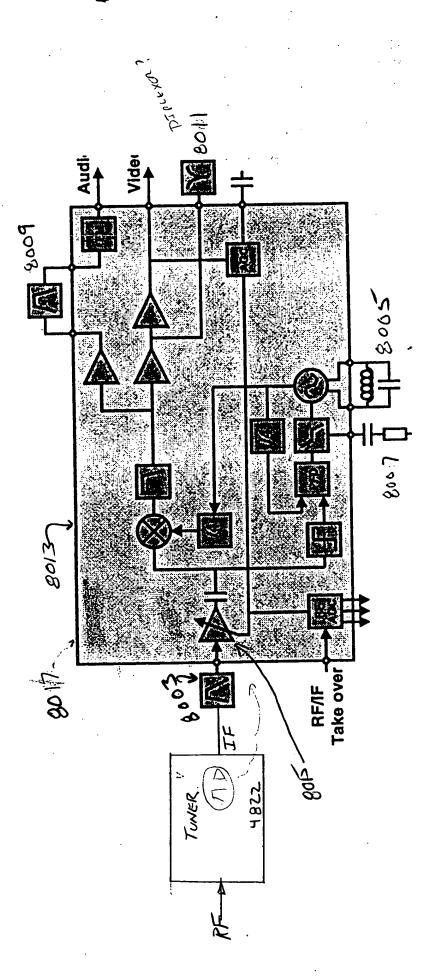


FIG. 8

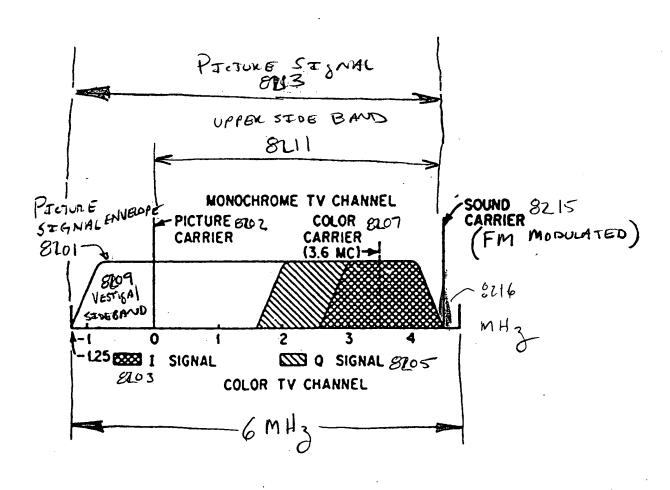


FIG. 82

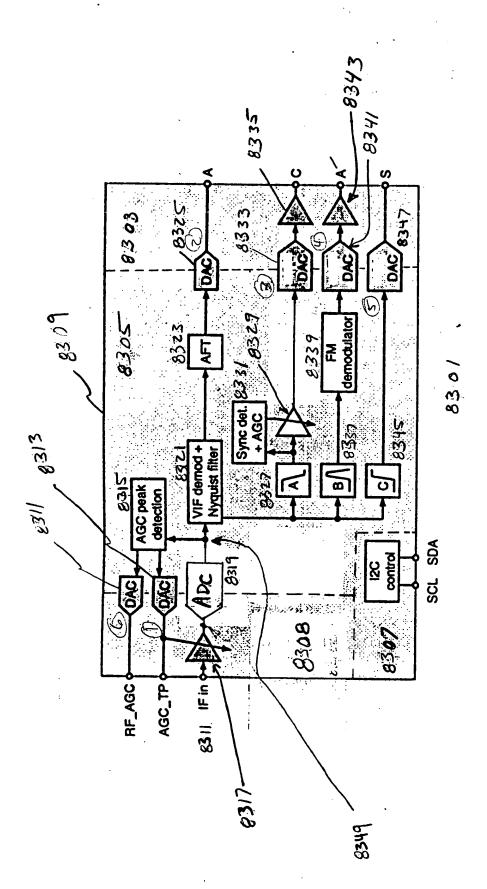


FIG. 83

